IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.,	(	CAUSE NO. 2:22-CV-293-JRG
Plaintiff,	)	
vs.	)	
SAMSUNG ELECTRONICS CO., LTD., et al.,	)	MARSHALL, TEXAS
Defendants.	)	SEPTEMBER 26, 2023
	)	8:30 A.M.

MARKMAN HEARING

BEFORE THE HONORABLE RODNEY GILSTRAP
UNITED STATES CHIEF DISTRICT JUDGE

SHAWN McROBERTS, RMR, CRR
100 E. HOUSTON STREET
MARSHALL, TEXAS 75670
(903) 923-8546
shawn_mcroberts@txed.uscourts.gov

A P P E A R A N C E S

FOR NETLIST:
IRELL & MANELLA, LLP - LOS ANGELES
1800 AVENUE OF THE STARS
SUITE 900
LOS ANGELES, CA 90067-4276
(310) 203-7096
BY: MR. JASON SHEASBY

McKOOL SMITH, P.C. - MARSHALL
104 E. HOUSTON ST., SUITE 300
MARSHALL, TEXAS 75670
(903) 923-9000
BY: MS. JENNIFER TRUELOVE

FOR SAMSUNG:
FISH & RICHARDSON, PC - WASHINGTON DC
1000 MAINE AVE. SW, SUITE 1000
WASHINGTON, D.C. 20024
(202) 783-5070
BY: MR. MICHAEL McKEON
MR. BRIAN LIVEDALEN
MR. CHRISTOPHER DRYER

FISH & RICHARDSON, PC - SAN DIEGO
12860 EL CAMINO REAL, STE. 400
SAN DIEGO, CA 92130
(858) 678-5070
BY: MR. FRANK ALBERT

GILLAM & SMITH, LLP
102 N. COLLEGE, SUITE 800
TYLER, TEXAS 75702
(903) 934-8450
BY: MR. TRAVIS UNDERWOOD

FOR MICRON:
WINSTON & STRAWN, LLP - REDWOOD CITY
255 SHORELINE DRIVE, STE. 520
REDWOOD CITY, CA 94065
(650) 858-6443
BY: MR. MICHAEL RUECKHEIM

WARD, SMITH & HILL, PLLC
1507 BILL OWENS PARKWAY
LONGVIEW, TEXAS 75604
(903) 757-6400
BY: MR. CHAD EVERINGHAM

OFFICIAL REPORTER: SHAWN M. McROBERTS, RMR, CRR
100 E. HOUSTON STREET
MARSHALL, TEXAS 75670
(903) 923-8546

THE COURT: Be seated, please.

All right. This is the time set for claim construction in the case of Netlist, Inc., versus Samsung Electronics, et al. This is Civil Case No. 2:22-CV-293.

The Court will call for announcements at this time.

What says the Plaintiff Netlist?

MS. TRUELOVE: Good afternoon, Your Honor. Jennifer Truelove here for the Plaintiff in this case. Joining me today and presenting argument is Mr. Jason Sheasby. We also have some client representatives out in the audience, Mr. Tobin Hobbs and Jayson Sohi. And we are ready to go, Your Honor.

THE COURT: All right. Thank you, counsel.

What says the Defendants?

MR. UNDERWOOD: Good afternoon, Your Honor. Travis Underwood on behalf of the Samsung Defendants. With me this afternoon are Mike McKeon, Frank Albert, Brian Livedalen, Christopher Dryer. And in the gallery we're also pleased to have two client representatives with us, Young Chun and Sunghun Lee. And Samsung is ready to proceed, Your Honor.

THE COURT: All right. Thank you.

MR. EVERINGHAM: Good afternoon, Your Honor. May it please the Court. Chad Everingham and Mike Rueckheim are here for the Micron Defendants. And we are also pleased to be joined by our client representative Becky Carrizosa. And we

are ready to proceed.

THE COURT: Thank you, Mr. Everingham.

All right. That should be all the announcements. Let's turn to the disputed claim language that's set for construction today.

Counsel, we've got a lot of ground to cover in the time allocated. I understand there may be an agreement that at least one of these terms should be taken up on the papers only and not subject to oral argument today. Is that correct, or am I mistaken?

MR. SHEASBY: Your Honor, Mr. Rueckheim, who is arguing 'circuitry' on behalf of both parties, indicated that he was prepared to submit on the record. Given the number of terms, I agreed to that as well, subject to the Court's approval, of course.

THE COURT: Is that correct, Mr. Rueckheim?

MR. RUECKHEIM: That's correct, Your Honor.

THE COURT: All right. Then we'll reserve 'circuitry' for resolution on the briefing and papers.

Let's start with 'memory module comprising' from the '912 Patent, with similar language from the '417 and the '215. Let me hear argument.

Let's begin with the Plaintiff on this one.

MR. SHEASBY: May it please the Court.

If I could have the slides.

There are two issues that I think are threshold issues. The first is there was some procedural argument that the claim construction positions are unripe because of the evolving nature of the dispute. And to put it in precise context, there is a part of that argument that is incorrect and a part of it that is correct. So there is a fundamental dispute about whether 'rank' can encompass one memory device, and that has been live since the parties first began negotiating the claim terms.

There are two other aspects of the discussion of 'rank' that became apparent. There was a live dispute as we reviewed the interrogatory responses and contentions and other matters that the Defendants have set forth. Those two other disputes are whether 'rank' has to be a defined set of devices or it can change on the module, and also whether 'rank' needs to operate with all chips in the module. It is, in fact, correct that those two issues are embedded issues that Defendants' claim construction does not seek to engage, but it is quite clear that there is a dispute of claim construction as to those two issues as well. And so we think discretion is the better part of valor in this situation and we should deal with it upfront.

THE COURT: So does that mean that in addition to whether the term 'rank' can be one or must be more than one, there is a live dispute, in your view, counsel, as to whether

the rank of devices corresponds to a fixed bit width. Is that still an issue?

MR. SHEASBY: It still is an issue, as is the issue of whether you need to read every device in the rank.

THE COURT: Okay. Whether or not a partial read is permitted.

MR. SHEASBY: Correct, Your Honor.

THE COURT: All right. Let me hear your argument on these issues.

MR. SHEASBY: Your Honor, 'rank' and 'DDR devices' are terms that appear in either -- 'rank' appears in all the claims and 'DDR devices' appears in the '912 claims in addition to 'rank'. And those are not terms that have some imaginary abstract reading meaning; those are terms that are actually created by JEDEC themselves. And so we know that the patents-in-suit are read in the context of JEDEC standards because the '912 Patent makes that clear. This is on slide 6. And we know --

THE COURT: So are you telling me the plain and ordinary meaning of 'rank' doesn't apply; that there's some special lexicography that comes out of JEDEC.

MR. SHEASBY: I would say the plain and ordinary meaning of 'rank' is JEDEC; in other words, that in the context of a memory module, the term was created by JEDEC. And the evidence of that is pretty substantial.

So if we look at slide 7, the term 'rank' was created by JEDEC, the memory industry standards group. This is what Micron has said publicly. And, of course, JEDEC began dividing the term 'rank' and using that term from DDR1 forward. So it was already well-established by that point.

THE COURT: So let me ask you this, counsel. Given the prominence of JEDEC in this situation, are we, in fact, dealing with patents that are standard essential, or are these patents somehow not standard essential, notwithstanding the influence of JEDEC?

MR. SHEASBY: So what I would say is the following: Is that these patents are built on top of -- if we go to slide 13, these patents are built on a baseline of JEDEC specifications, and then certain departures are made from JEDEC specifications in order to advance the field. So when they --

THE COURT: When they're built on that platform of JEDEC, do they take on the obligations of FRAND and other things that are applicable to standard essential patents, or does somehow the deviation from that once they've built on the platform, does that somehow insulate them from the obligations of fair, reasonable, and non-discriminatory?

MR. SHEASBY: Yeah. So these patents are a different species than the patents last time. For at least the '912 Patent, my understanding is the '912 Patent, the

ultimate contentions, and an expert will have to do this, is that it's actually essential; in other words, that it doesn't depart -- it was subsequently adopted by JEDEC. And so this would be a species of a patent that is not just built on; it's -- so at the time it was created, JEDEC had not yet standardized it. It was forward-looking as to what was going to actually be the case at DDR4. This patent reads on DDR4 and DDR3, but it was created long before that. But my understanding is that for DDR4, the '912 Patent is -- the experts are likely to find that it's actually essential; that it was fully adopted by JEDEC.

THE COURT: All right.

MR. SHEASBY: But the --

THE COURT: Let's get back to 'rank'.

MR. SHEASBY: Sure. So the -- so Doctor Stone I think addressed this for the purposes of claim construction. The patents are supposed to comply with JEDEC standards. And there's different levels of JEDEC standards. The JEDEC standards that these are compliant with are those relating to 'DDR' and 'rank'. And the specification--and Micron makes this clear--that in the context of JEDEC and in the context of DDR devices and memory modules, a rank is multiple DRAM components. And that exists for a very specific reason.

If we go to slide 11.

The width of a JEDEC device, the DDR chip, the width of a

rank in DDR is either 64 or 72 bits, and it's been that way since the beginning of the JEDEC standardization of the term 'rank' and of the term 'DDR'. And that has necessarily required more than one chip at all points in time. And so when you're talking about a DDR memory chip, which the '912 recites, when you're talking about 'rank', which the '912 and the other patents cite of necessity, you're talking about more than one chip. It's scientifically impossible for you to have one chip that's the bit width of JEDEC DDR, which is a term that only exists in the context of JEDEC.

The testimony of Harold Stone, this is on--I was on slide 9 previously; this is on slide 12 now--in which Doctor Stone makes clear again that in the past and present there has always been a requirement for more than one chip in a rank for DDR devices. And, of course, Micron's corporate representative makes clear as well that there's always been more than one chip required for a rank in DDR devices.

So 'rank' and 'DDR devices' don't have a plain and ordinary meaning in the sense that you would go to a dictionary to look them up. They were terms that were created by JEDEC, and in the context of JEDEC they have a plain and ordinary meaning, and that context is a rank is more than one DDR device.

So although I'm showing what may seem like extrinsic evidence, it's actually, in my mind, not extrinsic evidence

because the terms -- the patents actually use these sort of coin terms for JEDEC of 'DDR' and 'rank multiplication'. This is slide 14 where I'm showing the testimony of Mr. Holbrook.

I don't think there is a substantial attempt by either of the Defendants to engage this issue in their briefing; instead, they sort of suggest that the Court ignore it because they say that the specification contemplates a rank with only one device. I would respectfully submit that the other intrinsic record, in addition to incorporation by reference of the JEDEC standards, does not support that.

So if you look at the specification--I'm on slide 15--there is a repeated contemplation of the ranks having multiple devices. If you go to slide 16, you look at Figure 1A, and if you look at every figure in the specification, the rank is always described as having more than one device.

They have I think two arguments based on the intrinsic record as to why they think a 'rank' can have just one device. The first one relates to Table 1. This is on slide 17. Table 1 is referring to, if you look in the specification at 7:56 through 59, 'rank of memory devices' -- 'ranks of memory devices' plural, so it contemplates that there are multiple memory devices in each rank.

I'm on slide 18. This is I think their argument that, in my mind, I was I think the most unclear from the briefing on both sides. So they talk about this Logic State 4 as being an

example in which there would only be one device in each rank. And what they argue is because it said in Logic State 4 the command signal, e.g., 'read', is sent to only one memory device or the other memory device, and they imagine that that's a scenario in which the command signal is sent to only one rank or the other rank. In other words, there's two ranks that are -- there is two ranks available for the signal to be sent to, and one is -- only one is chosen.

But if you look at the specification at 8:26 through 62, you will see that that Logic State 4, there's only one rank available. So what the specification that they point to is actually describing is an instance in which there's one rank available, there's two chips within the rank, and read signal is sent to only one of those two chips. The confusion is that they imagine that State 4 is a state when two ranks are available, when, in fact, State 4, if you read the context, is an instance in which only one rank is available.

THE COURT: Let me ask you this, Mr. Sheasby. There's some mention in the briefing about Netlist having characterized 'rank' as being something with one device when it appealed an IPR decision, with the implication being there's either some kind of disclaimer or estoppel or something there. What's your view on that issue?

MR. SHEASBY: Yeah. I found that confusing. I think it's actually just the exact opposite. And this is just

a situation where I think there needs to be a careful reading of the opinions by the Central Reexamination Unit and then the Patent Trial and Appeal Board. This is on slides 19 and 20 in my deck.

On slide 19 -- 18, the -- we actually argued that the Amidi reference was not invalidating because in Amidi it only sent a signal to one device; whereas, in our system, our claim system, a rank required a plurality of devices, and it would not have been obvious based on Amidi, which sent a signal to only one device, to send a signal to only one device in which there are a plurality of devices in a rank.

And so, in fact, we argued just the opposite. We didn't argue that 'rank' could only have one device; we argued that Amidi was not anticipating because there were -- they -- it did not contemplate a plurality of devices in the rank; it was only one device could theoretically exist, and the signal was sent to that one device. Our patent has multiple devices in the rank, but there's a capability of sending it to only one device.

THE COURT: So are you suggesting that the Defendants misrepresented --

MR. SHEASBY: I don't think it's the misrepresentation. I think it's just a confusion in understanding the context. I think what Defendants thought when they read this quickly was that this was talking about

Amidi having plurality of memory devices. That's not actually -- it's just the context they got wrong. It's not Amidi having a plurality of memory devices, it's Amidi not having a plurality of memory devices; whereas, the claims require plurality.

And this is slide 20 as well in which requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to only one DDR memory device at the time when there is a plurality of memory devices in a rank. That's saying that Amidi, sending one signal to one device, did not render obvious sending one signal to multiple devices in a rank.

So I attribute no ill-will whatsoever, but I do think, with all due respect, there was just a confusion and a misinterpretation of the IPR.

Your Honor, with your permission I'll move on to some of their other arguments --

THE COURT: That's fine.

MR. SHEASBY: -- in the intrinsic record. And I want to focus on -- I don't think it does anyone any good to sort of not recognize that there are distinction.

The '912 Patent describes both 'DDR devices' and requires both DDR devices as well as 'ranks'. And in our mind that's the apogee of the warrant that 'rank' should be multiple devices as required in and contemplated by JEDEC.

I certainly understand that the other two patents are not limited to 'DDR memory devices', and that the basis for interpreting 'rank' as requiring more than one device would in that context be just the specification and the understanding of the word 'rank'. But I think even those -- in those other patents, there is robust amount of evidence that a rank does not contemplate one device.

I think their best argument in the intrinsic record is '215 Patent, claim 1. And what they say, and the PTAB noted this as well, it's -- by the way, the '215 is a completely different specification than the '912, and I'm not clear how this would be relevant to what's in the '912. But what it says is it talks about -- in some of the dependent -- some of the later limitations it selects out one first memory integrated device and one second memory integrated device a and a first rank and a second rank. And I think that the board on first blush, as well as my brothers, imagined that that means that a rank only has one device. But this is a situation in which the first and the second rank are -- first memory device and second memory device are being identified because there must be one device in each of those ranks that does something specific, and that is one device in each of those ranks must have connected to it a buffer that buffers it along. And this is on slide 25.

So I think in terms of the '215 Patent, claim 1, it's not

stating there's only one memory integrated circuit in the rank, it's stating that there has to be at least one memory integrated circuit that has the features that are listed below, which is a state that they are connected to a buffer.

I think that the other arguments that the Defendants make is they focus on claim 55 of the '912 Patent in which they say that each rank of a first number of ranks comprises a plurality of DRAM chip packages having a total bit width equal to the sum bit width of the DDR chip packages of the rank. This is slide 27. And they say, Well, this claim 55 requires a plurality of ranks and, therefore, claim 1, which it depends on, does not require a plurality of devices in a rank. And I think this is, once again, just -- it's a good faith argument, but I don't think it actually engages the issue.

The issue with claim 55 is not that there is multiple devices in the rank; the issue is that all the devices in the rank add up to a specific number of bits, a bit width length, and SO that has nothing to do with whether claim 1 requires THE -- whether claim 1 requires multiple devices in a rank.

The '912 Patent, claim 15, they also argue that the -- somehow the language in the claim itself contemplates one device in each of a rank. I think that that is -- I think it's hard to read that when you parse it correctly. So basically what they say is that if a memory devices was plural, it would -- in each rank, it would make this language

up here redundant, the language in the red underlining redundant. But what it's doing is claim 19 is -- claim -- the claims of the '912 Patent are doing two things. First, they are defining the type of memory devices--it's got to be DDR memory devices; second, it's saying that there are a number of those devices in each of a number of ranks, defining the physical ranks; and then there are a number of each of those devices in logical ranks defining each of the logical ranks.

So I think reading into this contemplation that an individual memory device -- that a rank can only have one memory device because if -- because of some argument that if it would -- if it required more -- the language I circled was redundant I think is a bridge too far because that language exists not to identify the number of memory devices, but identifies exist to define their nature.

And then I think the last argument they make is they point to Figure 6A and they say that 6A contemplates two separate ranks with separate devices. This is I think, is, once again, just a good faith confusion. There are two separate embodiments -- two separate concepts of strategies that are described in the specification. There is a set in which you actually combine two physical chips together to mimic the behavior of one chip, and there is a design in which you have two separate ranks which are logically mimicking the design of one rank. In Figure 6A and the specification

associated with that is not about ranks. It makes no reference to rank whatsoever. It talks about how to combine two physical chips to make them logically look like one chip, which is one of the embodiments, not the claimed embodiment.

Your Honor, that's the sum of my argument on the multiple rank issue. Would you like me to turn to the other two issues, or would you like me to --

THE COURT: I want you to do that, but before you do, I want to ask you for your response to the offer of extrinsic evidence from the Defendants from Bruce Jacob where he defines "a rank of memory is a bank of one or more DRAM devices." Why is he wrong when he says 'one or more' from this memory system cache DRAM disk publication from 2007? Why is that wrong?

MR. SHEASBY: So if you read the context of that, it's talking about an old system in which a rank is a bank of one or more DRAM devices. And because of that ambiguity in the sense that a DRAM -- a bank could be on an individual chip and an individual chip could have two separate ranks and each of those ranks there could be only one array of memory, what the -- it actually goes on to say it's "To lessen the confusion associated with overloading the nomenclature, the word 'rank' is now used to denote a set of DRAM devices."

So what he's talking about, there was an old usage before JEDEC standardization in which 'bank' and 'rank' were used

interchangeably, and it created confusion because on a chip -- an individual chip, a bank may only have one array or one set of devices on it. What he's saying is that now a rank is used exclusively to note a set of DRAM devices, which is multiple DRAM devices.

So in terms of Jacobs, I'm not running away from Jacobs, the Jacobs actually proves the point. There was an archaic sort of conflation of 'bank' and 'rank' that has -- that was sort of a pre-JEDEC design. That conflation has now disappeared with the JEDEC creation of the term -- formalized term 'rank' in the context of DDR devices, with the record 'rank' is now used to note a set of DRAM devices. The 'now' is speaking about the context of when the '912 Patent was issued.

And then, of course, if you go on -- I was on slide 22. I was complaining that on slide 23, now -- is that when they talk about this context of 'rank' now means multiple DRAM devices is, again, presented on slide 23.

So the Jacobs point and -- is in my mind just another situation in which you just need to read a little more closely than I think was done historically. There was an old definition of 'bank' and 'rank' that conflated them. There was a new definition of 'rank' that made it multiple DRAM devices. That was -- in terms of the contemporaneousness of the text, this language about the new -- the 'now', the 'now'

is the time of the '912 Patent.

THE COURT: Several times you've argued that the term 'rank' was a creation of JEDEC. Put me in the Garden of Eden. Show me the point of creation where JEDEC creates 'rank' as a term. Where did it happen? How did it happen?

MR. SHEASBY: DDR1. So at the time of -- when DDR1 was standardized, the bit width that would be used in modules was set at 64 or 72. And when that bit width was set at 64 and 72, the JEDEC made clear that JEDEC defined the term 'rank' as meaning multiple devices because it was theoretically impossible to create a device at 64 or 72 bits on its own, so the only way you could do it was by having multiple devices.

So it's -- Harold Stone talks about it in the DDR and DDR2 standards. This is on slide 11. The widths were defined as 64 and 72, and at that point that defined rank ineluctively is meaning more than one device because there was no single device that could have a width of 64 or 72, and, of course, Mr. Holbrook testifies to the same as well.

So once --

THE COURT: Do we have a document generated by JEDEC that says, Henceforth, we are using the word 'rank' to mean more than one device? Do we have something that precise, or is it just an evolution over the usage through DDR that we get to the position you've taken?

MR. SHEASBY: So it's -- so it actually -- so the most precise thing in the record is slide 7. This is Micron's testimony that Micron said -- reported that JEDEC created the term 'rank' and that that term required there to be multiple DRAM devices. But in terms of the most specific things in the record, at DDR1, the bit width was set at 64 for a rank and a module, and that was -- that's required and standardized, and that will be undisputed by Defendants. And at that point it was ineluctable that a rank would require more than one because the -- there is no such thing as a chip that has more than 64.

I can actually show you the specifications. They are in the record, Your Honor. If you give me one moment I will find them.

Slide 32, Ms. Truelove.

I'm on slide 32. This is the JEDEC DDR standard, which is Exhibit 7 and Exhibit 8 in our brief, Your Honor. This is for DDR1 and DDR2, and they both define the bit width as 64 and define the number of chips that would be in their rank, it would be either 4, 8, or 6 based on the size of the chips that are allowed under JEDEC.

THE COURT: 4, 8 or 16?

MR. SHEASBY: 4, 8, or 16, Your Honor. Excuse me.

THE COURT: Let's move on to the fixed bit width and the partial read issues.

MR. SHEASBY: Yes, Your Honor.

On the fixed bit width issue --

If you go to slide 37 -- 36, Ms. Truelove.

Sure. It's our contention that the memory -- that a rank is not some arbitrary logical structure that's created. The idea of ranks on the device are that they're physical structures with defined physical contractual metes and bounds. You see that on slide 36 from the specification at -- from the claim itself. And you see that in -- for example, in '912 it talks about the memory devices being arranged in a first number of banks. 'Arranged' is a physical act. It's not something where the rank can change arbitrarily over time.

Slide 40 speaks about the fact that --

I'm sorry. Slide --

All the claims themselves make clear that a rank is a physical construct. It's not something that logically changes based on some software or something. And you know that from the plain language of the claim which talks about the devices being arranged in a first number of ranks.

As to being able to send data from only a subset of devices in a rank, it is clear that you must have a capability to use every device in the rank, but I think any argument that every device in the rank must be used turns the specification on the head.

If you look at column -- slide 40, this is '912, 8:44

through 60 and 7:56 through 59, the whole point of this design is only to address a single memory device that would be in a rank. So this is State 4. State 4, one rank is turned on. And although there are multiple devices in that rank, you're sending it to only one or the other device in the rank. So it would be -- do violence to the entire purpose of the specification if you required every chip in the rank to be addressable.

And I think that that is supported by Doctor Wolfe, who's one of Samsung's experts who testified that it's still a rank if you do a partial read from it. In other words, one of the tactics in the patent is there to be partial reads. That's what 8:44 through 60 speaks about.

Oh, and there's one other issue that they talk about. There is a portion of the specification in which it talks about 32-bit width modules and 32-byte DRAM devices, and they say, Well, if you combine 32 and 32 together, it would be one chip and one sort of set of bit width, but that's not defining rank; that is just defining a theoretical option. If you didn't speak about ranks, if you didn't speak about DDR devices, you could create a crazy 32-bit -- 32-byte DRAM device and use it in a 32-bit width module, but that would not be a rank -- a JEDEC rank, and it would not be a DDR device, because DDR device does not standardize 32 bits.

Thank you, Your Honor.

THE COURT: All right. Let me hear from Defendants in response.

MR. McKEON: Good afternoon, Your Honor. Mike McKeon for Samsung.

THE COURT: Good afternoon, Mr. McKeon.

MR. McKEON: Nice to see you again. And lots to respond to there, so let me get -- just get right to it, if I can.

THE COURT: I expect this term to take most of the time.

MR. McKEON: This is a hotly --

THE COURT: Things should move quicker after this.

MR. McKEON: That is right, Your Honor. This is the one that's -- I think the parties are focusing on for this proceeding.

So I think a little context here, Your Honor. I mean, we're actually in a situation where we have the Plaintiff patent owner coming in and trying to lard this term up with a bunch of limitations to narrow the term, you know, including this issue of whether it covers one or more or that it has to be two or more. But what's going on here is we're at the Patent Office, as Your Honor knows, and the Patent Office has rejected this argument that the claim is limited to two or more three different times.

And let me just show you the timeline here. We filed an

IPR on the '912 before the lawsuit in this case was even filed. We filed that IPR in July of '22. The lawsuit was filed in August. And then we had an institution decision on the '912. And, frankly, there was some politics going on in the Patent Office. It was withdrawn from institution, and the director had to look at it again because of an issue regarding Google and whether Google was actually a party in interest. That issue has been resolved, and it was instituted again, the '912. Then the '215 and '417 were all instituted and they're all pending right now in the Patent Office.

So we have a situation where the proceeding in the Patent Office is going on in parallel, and the reason is because these things were filed so early. We're actually -- in the Patent Office they looked at this 'one or more' and rejected it three times.

And these other issues that are being presented here in the *Markman* hearing about these other limitations, they're trying to get this Court to -- well, pit this Court against the Patent Office. I mean, that's what this proceeding is all about with this term. It's an effort to narrow based on prior art.

Really, as far as we can tell, Your Honor, I'm not sure there are any infringement issues here or anything in this Court that's going to be relevant in terms of the claim constructions. It's really an issue of prior art and the

Patent Office.

THE COURT: So are you suggesting that this Court should just defer to the PTAB for purposes of claim construction?

MR. McKEON: Well, what I would suggest, Your Honor, frankly -- and, you know, as you know, we have a pending motion to stay pending IPRs, and three out of the four patents--the '608 Patent was just added--three out of the four are pending in IPR.

THE COURT: And the standard for claim construction at the Board is not the standard for claim construction under *Phillips* at the court, is it not?

MR. McKEON: No, it absolutely is, Your Honor.

THE COURT: Identical?

MR. McKEON: Identical. *Phillips* governs -- in the early days after 2011, in the early days they had this broad --

THE COURT: I understand that. But even after that was changed, are you saying it's on all fours with --

MR. McKEON: All fours in *Phillips*. *Phillips* controls the Patent Office now; absolutely, Your Honor.

And remember, Your Honor, another thing to keep in mind here on this is, of course the prosecution history is always relevant, Your Honor. So we're literally creating prosecution history right now in the Patent Office. I'm going to show you

some of it actually. So we're creating that. And, of course, that guides your -- that's intrinsic record and that's going to guide your evaluation. And the point is we're pitting that against this process. And it's an unusual case because we're so far along in the Patent Office, so that's why I think it's a little more unusual. You don't see that a lot.

THE COURT: Well, I don't intend to argue your motion to stay.

MR. McKEON: And I'm not trying to do that, Your Honor; I just want to give context here about why we have a situation where the Plaintiff is coming in trying to narrow this claim, and Samsung's been consistent all along here. And so let me just dive into that, Your Honor.

THE COURT: Please do.

MR. McKEON: And I'm not going to spend the time on -- you know, there was a procedural, we think, process, you know, with all respect, failure in the sense that we saw in the initial constructions a proposal by Netlist that really kind of matched what Samsung was proposing and -- in terms of they have a set of DRAM devices. They didn't have one or more, but it was a 'set' which, of course, a definition is one or more, 'acting together' was in their initial proposal, and 'in response to command signals'. The only dispute we had initially was this fixed bit width, and that was the initial position they took here, the Patent Office stuff moving

forward, and that's why today we have a different proposal from them, which is these issues that Mr. Sheasby just argued.

So that's sort of background here, Your Honor. And I'm going to deal with the -- whether Your Honor accepts that as a procedural flaw, you know, I'm going to argue all the issues and you're going to have that before you, but I think there is a procedural issue there.

Let's get to rank, Your Honor.

What I show here on the slide are the institution decisions for '912 and '215. And again, this is part of the prosecution history. And these are only the institution decisions so it's not final, but it's pretty compelling.

With respect to this 'rank' issue, "Patent owner does not agree with petitioner that a rank includes a single memory device, but does not otherwise dispute petitioner's rank construction," which, of course, is the construction that we're talking about here in this courtroom. So there in the Patent Office they didn't dispute it. The fight was 'one or more'. And that was the issue that was presented to the Patent Office, and they in every single instance agreed with Samsung.

And Your Honor, they agreed with Samsung based on the intrinsic record that was presented. That was really sort of their analysis. I'm going to go through that in detail. But what Mr. Sheasby has done here, he's turned everything upside

on its head. In fact, as far as I recall, he started his presentation with all this extrinsic evidence, and that's not where we start normally; we start with the intrinsic record. So he's trying to say that JEDEC governs here, and whatever's in JEDEC you should construe the patent that way. Well, Your Honor, I'm going to demonstrate to you that would be inconsistent with the intrinsic record, if you are going to say, Oh, JEDEC -- whatever happened in JEDEC, that's what happens in these patents. And I'm going to walk you through that now.

First and foremost, Your Honor, '215 Patent -- and Mr. Sheasby addressed this, but I think it's just worth highlighting. The claim in that patent actually claims at least one first memory integrated circuit in the first rank. So, in other words, we have a patent in this case, Mr. Sheasby wants you to say it requires two or more, but we have a claim that requires at least one. So a construction with 'two or more' would be in direct conflict with the actual claim language. So that can't be right. That argument can't be right.

And remember, these patents are all related. The '912, Your Honor, is the earliest, and they all go back to two patents. And the numbers I believe are -- '386 I believe is one of them, and there's a 4 something, Your Honor, but it's in the record. They are the great-grandparents. They all

flow from that. And the case law tells you that this 'rank' term should be construed consistently.

So I have a '215 Patent claim that the Court cannot construe 'two or more' because it would be in the -- it would be in conflict with the language of the claim where it says 'at least one'. So we know that's not right for '215, and we think you should construe them all together. 'Rank' shouldn't mean one thing for '215, something else for the other patents.

And the argument that Mr. Sheasby made, you know, he's focusing on the language 'DDR' that's in the '912 claim. And DDR is double data rate. Your Honor, this is a Samsung invention--double data rate. The fact that double data rate, that DDR appears in a claim and it's discussed in the patent specification doesn't link this somehow to JEDEC; not at all. Double data rate -- you can have different embodiments and implement a double data rate system, and I'm going to show you the excerpt in a minute here from the --

THE COURT: So is it your view that we're dealing with standard essential patents here or not?

MR. McKEON: Well, your Honor, the million dollar question we get. Right? And just like the last case, Your Honor, where we couldn't even utter the words 'JEDEC', as you remember, in the last trial, because, you know, Your Honor said, Hey, listen, this is off limits, no one saying it's standard essential. And now, of course, Mr. Sheasby comes

into court and he's hanging his hook on JEDEC. And I guess he does a concession here in open court that '912 is standard essential.

You know, we believe there's no infringement in these patents, Your Honor, and, of course, we believe the patents are invalid and they're on -- the patents are on life support in the Patent Office, Your Honor. I mean, these patents are on life support. So we think they're invalid, but we --

THE COURT: Do you speak for the Patent Office?

MR. McKEON: Well, I mean, I look at the record, Your Honor. You know, I look at the record. And, you know, institution was done on all three patents, and it's not final for sure and things can change, certainly, but, you know, that's the context of what we -- where we're debating this.

So I think the standard essentiality question, Your Honor, of course, is still -- I think the jury's still out on that, so-to-speak. I know -- I take Mr. Sheasby at his word that '912 is standard essential, but what we know for the purposes --

THE COURT: We're going to get to the bottom of that issue long before we see a jury in this case.

MR. McKEON: Yeah. Your Honor, I imagine that we would, just like in the last trial, you know. But what role JEDEC plays, Your Honor, is obviously going to be dependent on what happens here today, because Mr. Sheasby's telling you to

hook these things around JEDEC, and that's what he's saying, and we don't think that's right. We think that's all extrinsic evidence, has no place in this claim construction process.

THE COURT: Let's talk about extrinsic evidence for a minute.

Part of the extrinsic evidence that you cite in your briefing is this work by Bruce Jacob, and the quoted section of it about 'rank' says "a rank of memory is a bank of one or more DRAM devices that operate in lockstep in response to a given command."

MR. McKEON: Yes.

THE COURT: How does one device operate in lockstep? You have to have two devices to operate in lockstep with each other.

MR. McKEON: That's true, Your Honor. And the reason --

THE COURT: So can you clarify what this means?

MR. McKEON: Yeah. First of all, what I'll say is that on this article -- on this book, Mr. Sheasby was saying -- well, he came -- he started the argument with 'rank' was invented by JEDEC; then he comes in and he says, Well, Jacob is dealing with an old system about 'rank'. So I'm not sure where we stand on who invented what here. But what I can tell you here is that in terms of Jacob--and this is a book that

both parties point to--he's very clear on this, that it can have one device. And this is extrinsic evidence for sure, but if you have two or more -- if you have two or more, then, of course, you're going to have a lockstep situation where they're all going to act together.

THE COURT: Well, this doesn't say, If it's two or more, it operates in lockstep; it says "one or more devices that operate in lockstep," and I don't know how one device operates in lockstep.

MR. McKEON: I mean, Your Honor --

THE COURT: It takes two to tango.

MR. McKEON: Yeah. I mean, what -- just heading back to the patent a bit, I mean, one of the things the patent achieved or attempts to achieve is you have a memory -- you're communicating with a memory controller and you want to communicate with more than two ranks. So the goal of the patent was to have logic circuit that -- where the memory control would only see two ranks, not four ranks. And that goal is achieved, that very goal is achieved even if you just have one memory device in a rank, because you're still -- you can expand the number of ranks. So it's very consistent with the patent that you have one.

And let me show you this, Your Honor, because I think this, frankly, is compelling. Mr. Sheasby addressed it, but I'd like to walk you through it because --

THE COURT: I'll be glad to hear your version.

MR. McKEON: Yeah. This here, Your Honor, is telling. And what are we showing here? Mr. Sheasby says, Oh, this is all JEDEC. JEDEC doesn't make 32 -- JEDEC -- the JEDEC standard doesn't deal with 32-bit wide memory devices. It's 64 or 72, as Mr. Sheasby said. But look what we have here in the very disclosure of the patent. We have memory modules that have 32 bits--that's the width. And then we're going to have memory devices, and the memory devices in the rank can be 32 bits. So what does that mean? Well, that means you have the module is 32 bits, my rank will be 32 bits, and if I have a 32-bit memory device, what does that mean? That means I only need one.

And this is the disclosure in the patent, the intrinsic record specifically dealing with the idea that you can mix and match this to have a 32, 32; I'm going to have one chip, I don't need anymore. And as Mr. Sheasby said, that's not JEDEC. That's not JEDEC at all.

So the patent contemplates non-compliant/JEDEC compliant devices. And this is -- right here on slide 21 makes that compelling. It says 4 bytes, which is 32 bits. It's very explicit with 32 bits. That can be built -- you can build a device within the meaning of this patent and have -- by the very specification have one device. And I think that's a compelling point, Your Honor.

I do want to mention this claim 55, if I can, because I think that's another claim where -- the '215 Patent we already showed you the language; it says at least one. But here on claim 55, we have "each rank of the first number of ranks comprises a plurality of DDR DRAM chips." So, in other words, it's a -- this is a -- claim 55 is a limiting claim dependent on claim 1 where they -- they're explicit about plurality.

And again, you know, claim differentiation, why are we limiting that if the broader claim already covers plurality, and that -- and I think that's another persuasive point, Your Honor, to keep in mind.

Let's talk about Table 1. Mr. Sheasby spent some time on that. And we definitely have a different view of Table 1 than he does. And maybe it's misunderstanding on both sides. I don't -- you know, I don't think so. But we view Table 1, Your Honor--and the Patent Office actually explicitly considered this--but Table 1 is a description of how you're going to issue commands to these ranks and you're going to do a selected rank. And what it says here, if you look at the '912 language, and it's in both sets, the language, "A command signal"--which is in this case a read--"is sent to only one memory device or the other memory device." And if you look at the signals in Table 1, it only selects -- it will select a memory device, and it only -- it doesn't give you any signal that's going to select a memory chip within the rank. So the

Table 1 only talks about selecting a rank, not a chip within the rank.

So what does that mean? That disclosure there doesn't -- isn't talking about selecting the individual chip. And the language "a memory device or the other memory device," it's talking about two different ranks.

And I'm going to show you here, this is the analysis the Patent Office gave, because this argument was made at the Patent Office. In these -- the proceedings in the Patent Office with the pending IPRs this is what they said. "Rather, the passage quoted above indicates an embodiment in which each rank has one memory device." That's how the Patent Office viewed Table 1. Very consistent with what we've been saying in our briefing is what the Patent Office says.

And so there's no confusion, Your Honor, from my point of view from our side on this. I think it's very clear we're very consistent with the Patent Office who instituted this and came to the conclusion that one is right there in Table 1; it's one chip per rank.

And Your Honor, let me address this figure here that Mr. Sheasby addressed. Mr. Sheasby tried to, you know, argue that it should be set aside because it doesn't deal with the word 'rank'. Well, true, the word 'rank' isn't in this disclosure here with respect to 6A, but, of course, the patent is riddled with 'rank' and the whole invention surrounds the

idea of organizing here with ranks.

And if you look at what we show here and what's described in the -- in slide 25, you have -- the data lines here are in the -- I guess it's pink. These are the data lines. And they're all connected to the same pin. And what the description tells you is that you have memory devices A and B. So the debate here is, is that one rank or two ranks.

Mr. Sheasby says it's not relevant to 'rank' at all. But this is actually showing two different ranks with one chip in each rank, and the reason we know that is because it's connected to the same pin. So if I was going to have a read operation where these are of the same rank, I would get this, which is a collision. It can't be possible or these pins -- this pin connects these two memories. These have to be separate ranks, which is consistent with everything we're saying, consistent with the Patent Office's view on figure -- on Table 1 that we have these two different chips. It's explicitly disclosed.

Now he -- Mr. Sheasby is absolutely right, Your Honor. If you look at the figures, there is multiple chips in the rank. I mean, we don't dispute that, and that -- there's a lot of embodiments where they have that. Our point is there's embodiments and description that show you one. And there's embodiments that say you're not JEDEC, you have nothing to do with JEDEC, which I just went through.

And that's the issue is, is claim -- should you narrow the claim, as Mr. Sheasby wants you to, to only apply to two or more, because that's a narrowing -- he's inviting you to narrow the claim. And we think in light of the intrinsic record, Your Honor, you shouldn't do that.

There's some prior art, Your Honor, that's cited --

THE COURT: So this is all really about validity.

MR. McKEON: All about validity.

THE COURT: When a defendant wants it to be broad and not narrowed, it's about validity --

MR. McKEON: Right, Your Honor.

THE COURT: -- and when the plaintiff wants it narrowed, it's about validity.

MR. McKEON: Your Honor, you've done this enough where I think you know how that works.

THE COURT: Okay.

MR. McKEON: And the question is who's got the goods.

THE COURT: That's what we're here to find out.

MR. McKEON: That's what we're here to find out.

And, you know, we think, Your Honor -- you know, our focus really, Your Honor, we're trying to focus on the intrinsic record, you know, because I think in this case it is quite compelling. And again, this slide 27 is more evidence. This is in the citations in the '215 Patent showing

you one memory device per rank.

Now, let me address this. Mr. Sheasby dealt with it. Again, this is a -- some terminology, Your Honor. Google has a case with the '912 Patent that's at issue, and there was a re-examination, an *inter partes* re-examination. And sometimes people say IPR, but technically that's not really an IPR; it's an *inter partes* re-examination. There is a different process where you can amend the claims and all that. This stuff I'm showing you now is from that Google re-exam. It's not from the IPR or the *inter partes* review that's happening now.

So the Amidi reference that Mr. Sheasby referenced, that was all part of this Google re-exam. And what happened there is -- in fact, again, I have to take issue with what Mr. Sheasby said, which is Amidi has two or more chips, not one. It has two or more. And what the Patent Office is saying here is that there was no disclosure in Amidi -- claim 16 requires you to pick only one of the two. And the Patent Office -- like Amidi has two or more, and there is no disclosure of only picking one; therefore, we're going to allow the claim. That was the issue. And the language you see here is language where it says, "when there is a plurality of memory devices in the rank." So they said you have -- there's nothing in Amidi that says only one DDR memory at a time when there is a plurality of memory devices in the rank. And the point here is, their view of the claim at the time was

that you could have multiple because why would they -- I mean, in terms of how they analyzed Amidi, because Amidi had the two. So they said that when there is a plurality of memory devices in the rank --

THE COURT: They being?

MR. McKEON: The Patent Office. The Patent Office. There is -- why would you need to specify when? Why would you even make that statement if the patent claim is limited to a situation where you had to have two or more? What they were saying was it had to be -- you know, when you have that situation, then you've got to have disclosure that you're only selecting one.

And so this history from that Google *inter partes* re-exam, Your Honor, I think helps our side and really undermines the argument that somehow that this supports the two or more. I just think that, Your Honor, they are simply misreading Amidi because, again, in our view, it has two or more chips.

THE COURT: Why don't you give me your view on the fixed bit width issue and the partial read issue.

MR. McKEON: Okay. Let me -- just one quick thing about the JEDEC standards, Your Honor, if I may.

So JEDEC, you know -- as you know, Mr. Sheasby cites the JEDEC a lot, but this is all -- you know, I just want to make it clear that our view this is all the intrinsic record, and,

you know, there's nothing in here that compels a construction of this patent. And I think that's an important point to keep in mind.

But let me jump, if I can, Your Honor -- oh, yeah. That's slide 33, Exhibit 14 and 15 we were talking about. The '523 Patent is an unrelated IPR, and the JEDEC proposal cited on slide 15. And slide 16 actually goes into the disclosures, and you can see here that the disclosure of 'rank' here is a set of memory devices, which is consistent with what we're saying, and a collection of SDRAMs, which is consistent with what we are saying, a collection of one or more.

THE COURT: So you're saying the word 'set' must mean more than one.

MR. McKEON: I think that most people would say that, Your Honor, 'set' is -- could be one. In a mathematician point of view, 'set' can be one or more. Our construction, as you know, Your Honor, we put in 'set', you know, one or more, to be very explicit on it. That way we don't have any problems down the road about what we're talking about.

Your Honor, let me jump to your other issues real quick, but can I comment on Doctor Stone?

A lot of testimony from Doctor Stone. Doctor Stone was a Micron expert witness that presented a declaration in the Micron IPRs. And Mr. Sheasby deposed him. He gave no --

nothing in the declaration about 'rank'. There was -- he gave no opinions on that. And like a third of the deposition was, you know -- our friend Mr. Sheasby is very, you know, good to get to the issues that are important to him. A third of the deposition was on 'rank'. It wasn't something that he gave an opinion on. So that's the context of the testimony you see.

And if you read the other parts of the testimony here, you know, he believed -- this is what he says. "I believe that many definitions, in fact, competing and inconsistent definitions exist for 'banks' and 'ranks'." So that was his view at the time of the definition -- at the time of the deposition about these competing definitions. Of course, the one that we're concerned about, of course, is the one that applies to this patent.

And he repeats this, Your Honor. "I have not been asked to opine on 'rank' or 'bank' or the meaning of 'rank' in this patent, so I would have to review the materials and determine what they mean by 'rank'."

So Doctor Stone, Your Honor, I think you can discount what's been said about -- you know what Mr. Sheasby quotes on Doctor Stone's deposition. He wasn't there for that, he never gave an opinion on that, and he even admitted that, I got to look at this and think about it.

All right. So let me get to fixed bit width, Your Honor. This is actually I think pretty straightforward.

There is nothing in the patents that describe the bit width as fixed. It's just -- you don't find that. It's just -- you know, they have generally -- generally have a bit width, but there's nothing in there limiting it to something that's fixed.

This applies also to the extrinsic record, including the Jacobs book. Nothing in there -- and the JEDEC materials that Mr. Sheasby cites. Nothing in there about this being fixed. Nothing in the JEDEC materials about that, that -- the word 'fixed'.

And we do see actually a disclosure in the '912 Patent, "the number of memory devices of a memory module can be increased by increasing the number of memory devices per rank." So this idea that we can expand, it's not fixed, it can be increased, again, that's right -- this is slide 40, and that's right in the disclosure. It's not fixed. You can expand that.

So we think there's a problem with that just on the -- looking at the intrinsic record, and even extrinsic record that Mr. Sheasby relies on there's nothing in there about it being fixed.

So let me now address, Your Honor, the other arguments, the pre-determined argument.

I think, you know, part of our problem with that, Your Honor, is we don't know what -- when it says -- when

Mr. Sheasby says 'pre-determined', we're not sure what he means by that. Is it, you know, before I ship the module; is it before I put it in the computer; before I issue a command; before I issue a re-command--pre-determined when? And so, again, this is another word.

And I can tell you, Your Honor, the 'fixed' issue, the 'pre-determined' issue, just like the 'one or more' issue, is all about the prior art. That's what's going on here.

And again, we don't think that there is intrinsic to support for 'pre-determined'. And we do also think there's a problem just of how -- what does it mean in the context of the -- of this patent.

And as we cite here also, Your Honor, on slide 44, you know, their reply brief. And again, you know, they don't shed light on -- in any of their materials here what do they mean by this 'pre-determined' and when the determination is made. So really we're interjecting not only something that's not supported by the claim language or the intrinsic record, or the extrinsic record for that matter, but we just think it's ambiguous; you know, pre-determined when. And that's going to be a problem later on if the Court goes down that road. And again, no mention in the JEDEC -- this idea of being --

THE COURT: What's your view on whether a rank of devices can allow a partial read?

MR. McKEON: Partial read. So, Your Honor, we think

this -- that that limitation certainly is not required in the patents. Again, no -- nothing saying partial read or something less than a full read. You know, we do cite this lockstep concept. We cited that in our briefing. And Your Honor already pointed that out that these devices we're talking about having these ranks, memories, are operating in lockstep, and then standards, of course, as well; you know, in the standards we have --

THE COURT: Can you explain to me how one device can operate in lockstep?

MR. McKEON: Well, that was a question you asked earlier, Your Honor, and I think in that language -- you know, with that language, there's sort of -- it's broader in the sense of it will cover a two or more situation, because lockstep you need two. Right? But, on the other hand, Jacob was very clear that if you have one device, you know, in that sense, Your Honor, it's in lockstep with itself. Right? It's -- you know, it's --

THE COURT: That's my point. How can you in lockstep with yourself?

MR. McKEON: Well, in a design where you have the one--right?--which Jacob says that's known in the art, having one --

THE COURT: But Jacobs doesn't say 'rank of memory is a bank of one or more DRAM devices that when you have two

or more can operate in lockstep'; he says 'that operate in lockstep'.

MR. McKEON: Yeah. And Your Honor, we recognize that tension there, and, you know, again, I think Jacobs is extrinsic evidence, and I think --

THE COURT: I understand he's extrinsic evidence, but as you pointed out, but both sides rely on it.

MR. McKEON: Both sides do, and we concede that. We obviously like the statement about the one or more, and -- but there is some tension there with the lockstep. We concede that, Your Honor. But I think, you know, it's a textbook and it's really just sort of talking generally about these systems. And I think, you know, that's a situation where there would be two or more, because otherwise it wouldn't make -- it wouldn't be quite clear.

Then, finally, Your Honor, if I can, the DDR -- as I understand, there's -- Mr. Sheasby wants to -- we understood from the briefing at least--and I wasn't clear from today's argument, and maybe we can get some clarity--but the DDR memory device is -- is the intention to lock sort of the DDR memory -- the DDR references to the time of the invention, the 2005 time period? Because as I understand the argument, if we're supposed to look back to the time of the invention and we're going to look at DDR and look at the JEDEC specs in particular, well, then we have a problem, Your Honor, because,

of course, the infringement case is accusing -- they're not accusing DDR1 -- we're not going back to -- all the way back to there. And in an infringement case, particularly in the '912 is dealing with DDR4. So that spec wasn't around.

So when we lock it in, okay, are we going -- if Your Honor locks it into the DDR spec on the JEDEC, are we going to lock it into 2005, and then does that mean that DDR4 is not covered because we've locked it in?

So there is some -- and I don't know the answer. Mr. Sheasby hopefully can clarify that, because that's -- if you take his presentation to its logical conclusion, I think that's where you end up. And in that case we can, I think, all go home because then there's no infringement in this case because all the accusations are focusing on the later standard.

So that's one problem we have with it, overriding problem, but also in addition to the other things that I mentioned earlier about how -- you know, double data rate memory is a term of art and it's not -- there's no necessarily linking it to that particular JEDEC spec or JEDEC in general. And I think -- you know, Samsung invented it.

All right. With that, Your Honor, unless you have any questions on anything, I will turn the podium.

THE COURT: All right.

MR. McKEON: Thank you.

THE COURT: Thank you, Mr. McKeon.

Mr. Sheasby we've spent an hour on this first term and we have three hours for the entire process. Let's see if we can button this up and move on.

MR. SHEASBY: I'll do it very rapidly.

One, Mr. McKeon is both correct and incorrect--in other words, that the *Phillips* standard does apply in the PTAB, but where he's incorrect, and I think -- is that the PTAB issues what it calls a preliminary claim construction, which is actually not binding and can change. In addition, the PTAB is not governed by *02 Micro*, and the PTAB is not required to construe a term; it can just say the construction is irrelevant to my analysis.

And so to say *Phillips* governs in both, it's actually not accurate to say you -- Your Honor applies the same standard. Your Honor is held to a much higher standard by the Federal Circuit based on *02 Micro* than the PTAB is, just to correct what Mr. McKeon said.

The second point is we should go to the intrinsic evidence, and I agree with that. So this is the intrinsic evidence. This is the only portion of the specification for the '912 Patent that they said contemplates a rank with one device on it. And what it talks about in Table 1 is it talks about a tool for selecting ranks.

So these are the command signals that select ranks. And

this is in column 7, lines 55. And they talk about that Logic State 4. That Logic State 4 selects a given rank. Then after the Logic State 4 selects a different rank, then there is another set of command signals that can go in. If you read the specification, you'll see that there's also discussion of chip select signals. And so a chip select signal will then go in and specify a particular memory device within the rank.

So we are absolutely fine being bound by what's in the specification. Every example of the specification is a rank with multiple devices in the '912 Patent.

As to the '215 Patent, the claim is an entirely different claim, and this would not govern the '912 Patent. But what Mr. McKeon did is he split up the definition of what must be on the device, a first and second rank with multiple devices, from the idea of selecting one device in each of those ranks to perform a buffer -- so that it is attached to a buffer.

So I don't think that the language in the '215 Patent claim has any control over the '912 Patent, and if it did, I don't even think it would support what's in the '215 Patent. This is obviously a very important issue for Netlist.

I should just add, as to the Jacob text, you know, the Jacobs text -- and this is I think one of the dangers of the extrinsic evidence. The Jacob text talks about historically one device being in lockstep, and you have to ask yourself the question how can one device be in lockstep.

If I could have the slides. And actually let's take those down. I'll just speak.

It talks about -- this is slide 23. It talks about an old -- 22. It talks about an old use of 'rank' which meshed it with 'bank', but then talks about 'lockstep', but then it talks about the current definition of 'rank', which is a set of DRAM devices. And I didn't hear anything from my brother disputing that in terms of the vintage of Jacob, the '912 Patent is a time of the current understanding of 'rank' not the --

THE COURT: Let me ask you this, Mr. Sheasby. Give me your take on Mr. McKeon's argument about Figure 6A in the '912 and his argument that implementing your position creates some kind of a collision I believe is the word he used. Respond to that briefly for me.

MR. SHEASBY: Yes, Your Honor. I think I can respond to it in two words.

Figure 6A is an embodiment of linking together two devices, not linking together two ranks.

THE COURT: All right. Anything further?

MR. SHEASBY: No, Your Honor.

THE COURT: Okay.

All right. Let's move on, counsel and cover the remaining of these terms. Also, just for clarity in the record, I want to clarify something. I called -- at the

beginning of today's claim construction process, I called the Netlist/Samsung case; I did not call the Netlist/Micron case, 2:22-CV-294. Obviously this is a claim construction process that applies in both cases, and Mr. Everingham was kind enough to announce for Micron even though I didn't ask for a specific announcement. But I want the record to be clear that the process we're involved in now is relating to both cases for purposes of claim construction, and that's my oversight for not being clear when we started.

Okay. Let's go on to 'signal' and 'row'. And address 'signal' from the '912 Patent, please.

And Defendants have offered a specific construction; Plaintiff has argued for plain and ordinary meaning. Let me hear Defendants with regard to their specific construction first and then I'll hear from Plaintiff.

MR. McKEON: Thank you, Your Honor. Mike McKeon again. And let me direct you to the slides.

So yes, Your Honor, it's plain and ordinary meaning from Netlist, but if you look at the briefing, what we're -- what's going on here is there's a bunch of things going on in the plain and ordinary meaning that we don't think is appropriate.

And what we've done -- what Samsung has done, Your Honor, is we've adopted -- for the construction of 'signal', we've adopted the definition that's been Netlist's definition for years and years and years before this case, and I'm going to

walk you through that.

We've adjusted slightly the row/column address signal because, of course, we want to account for the row and column address language. It's a particular type of signal. So the broad definition of 'signal', 'varying electrical impulse that conveys information from one point to the another', row/column address signal is a particular type of signal, and so the information there--we're just being explicit in the definition--is an address of either a row or a column memory location, but otherwise conceptually --

THE COURT: Isn't this being framed for the Court on the basis of some disclaimer?

MR. McKEON: Let me walk through that.

THE COURT: Okay.

MR. McKEON: Okay? And this is, again, a timeline. And when you we look back in 2009, Your Honor, what happened was there is a *Google/Netlist* case, and it was regarding the '386 Patent, which is the -- was one of the grandparents to all the patents at issue here, other than the '608. And the word 'signal' was a disputed term. And the court construed the 'signal' term the way we're construing it here. That was the court's conclusion in the Northern District of California.

Netlist -- in 2010 Netlist--and this is slide 54--agreed to that construction in the *Netlist/Google* case. This is 2010. And then also Netlist in 2010 -- October 2010 submitted

that agreed construction, submitted to the Patent Office in an IDS.

So there's three things that Netlist has done sort of to firm up what it believes the word 'signal' should mean to one of ordinary skill in the art, and now it's changing its view on that. And let me just walk through some of the basic facts here, Your Honor.

This is the -- the construction as you see here on the slide here, this is what the court held. And this is back in 2009. And this is exactly how we're construing it. So we're very consistent with what the court held. And then if you go here on slide 56, this is the agreed-upon construction that Netlist agreed on in the *Google* case. And again, this was in 2010. And again, Netlist at this point agreed that this construction for the '912 Patent should apply. 'Signal', 'a varying signal impulse that conveys information from one point to another'.

Then Netlist took -- later took that construction, again in the '912 IDS, and submitted it to the Patent Office with that construction in it. And this was part of that re-examination proceeding I mentioned earlier.

Now, this case, Your Honor, we think controls the outcome here. This is the *Golden Bridge* case we cited in our brief. They didn't respond to it in their reply brief, so there's no response from them on this. And really the facts are just

like we have here--they submitted a construction to the Patent Office in an IDS, and the Federal Circuit says, Well, you're stuck with that; that's the construction. And, you know, they -- Golden Bridge, of course, said they never notified the PTO they had wanted a different meaning, so this is binding on them. And we think that result applies here, Your Honor. It's the construction they had since 2009, and now what they're saying is what we have here on the slide 59.

THE COURT: Let me ask you this. Language to which Netlist previously agreed, as I see the circumstances, did not resolve a dispute as to whether 'signal' could be packetized. And if it related to a different dispute, why is it disclaimer here?

MR. McKEON: Well, Your Honor, why are we going down the road where we're -- again, this is prior art. Okay? This is all about prior art. We have two things--packetize and dedicated lines. All of the sudden now here we are in this court and now we're dealing with packetized and dedicated lines, which is something that wasn't even part of the construction earlier.

Now, I view that as being inconsistent. You know, now all of the sudden we're trying to have a new definition. They say plain and ordinary, Your Honor. That's not their goal here. Plain and ordinary is for Your Honor to say that the claim requires dedicated lines and that the signal can't be

packetized. That's what their goal is here, if you look at the briefing. So they say plain and ordinary, but what's going on under that is an attack on the prior art, and that's why they want to have those two limitations, and we don't think -- we think it's inconsistent with what's happened prior to today in the Ninth Circuit and in the Patent Office, and we think it's inconsistent with their intrinsic record. And this is --

THE COURT: Well, I mean, my point is you're going back in time and saying this is the position they took and they took this position again here and we took this position again here but now they're taking a new position, and my question is, if those earlier positions were addressing an issue in dispute that's not in dispute here, then how are they somehow bound or have disclaimed the ability to take that different position with regard to a new dispute that wasn't an issue when they took their original position? That's what I'm trying to figure out.

MR. McKEON: Well, I mean, I would just characterize it a little differently, Your Honor. The dispute they're having is in the Patent Office, and they're trying to use this Court to influence what happens in the Patent Office. That's really the dispute that's going on here. And I think the word 'signal' is -- is the word 'signal' changing definitions? It's a very explicit technical point, and all of the sudden

we're going to change the definition that --

THE COURT: Well, I don't want to -- you know, the Court doesn't want to put its head in the sand about what may or may not be going on in the Patent Office but, by the same token, when Congress created the American Invents Act, they consciously created a parallel process. That doesn't mean that the district court controls the PTAB or the PTAB controls the district court. They're in parallel. So I've got my path that I've got to go down, and the PTAB's got their path they've got to go down, and perhaps we're looking at some of the same or similar issues, but what's going on in the Patent Office shouldn't be, at least in my view, the driver for how the Court discharges its obligation to construe the claim language pursuant to the proper standard.

MR. McKEON: Your Honor, I don't dispute that.

THE COURT: I mean, I don't want to ignore any practical realities here, but the governing process here is not about this is the strategy they're pursuing in the PTAB and that's what ought to force you to go down this different path in the district court. I don't think that's the right way to approach it.

MR. McKEON: I'm not suggesting that, Your Honor. I know Your Honor has very specific views on this, and my only point there is when we're building this intrinsic record, because it is part of the intrinsic record in the Patent

Office, we can't be blind to it; you know, we have to pay attention to it. And also, Your Honor --

THE COURT: I'm not saying be blind to it, but I'm saying not be controlled by it.

MR. McKEON: Right. And -- but I would also say, Your Honor, I mean, remember, part of the AIA was, you know, we wanted to add some efficiency to the process. You know, that was part of it, and --

THE COURT: How's that worked out for you?

MR. McKEON: Well, Your Honor, we all have different views on that. But now we're having these two processes, and at a minimum it's not efficient, you know, and I think that's one of our viewpoints.

But Your Honor, let me just direct you to this slide 59, because I think this is very compelling and goes to the point you're making on what they said before.

In the prior case, Google made the argument -- this is Google's argument, this is their brief, and they say, "Google seeks to improperly limit the scope of 'signal' to information presented on one or more pins of a device dedicated to that specific information." So this sounds familiar, Your Honor. This is the argument they're making here in this court. They want you to adopt this idea that it's dedicated. And they said to the Northern District of California that this argument is wrong and you shouldn't adopt it, and now they're here in

this court telling you to adopt it. You know, and this is the point is the signal is a signal.

And one thing they can't do, you know, is have a direct statement in the Northern District of California and then later in this court have something completely the opposite. I mean, that can't be right as a technical matter. And that's why I bring up the Patent Office, because I just want to give you an insight of what's on here and that's why these arguments are being made, even if they're directly inconsistent.

And then just a point on the actual substance of the argument, Your Honor. Of course there's a difference between electrical connections, you know, physical connections, and the signal that travels over the connection, and the specifications in '912, you know, is clear on that difference. And we have cites here on slide 61--you know, we have a connection, and then, of course, we have a set of control signals that are going over the connection.

We do cite some dictionaries, Your Honor, on slide 62. That's in the briefing.

Let me deal with packetized. So the packetized argument, this is what they say in their reply brief, and I was very cures about this. It says, "Packetized information transfer is not an electrical impulse, a high or low which translates into a 1 or 0, but is, instead, a group of 1s or 0s linked

together." So what it's saying is 'packetized' is a group linked together.

Well, first of all, we have the disclosure here where we have a signal line, so we have a signal going over the line, so where it repeatedly discusses data signals. But more to the direct point, Your Honor, we have in Figure 4A -- this is slide 65. What we've shown here is a group, a group of 1s and 0s all together. This is Figure 4A of the patent, the '912 Patent. And Mr. -- the -- Netlist says in their briefing that, Well, wait a minute; if it's a group of 1 or 0s, that's a packet. Well, that means they're excluding Figure 4A. If you adopt this construction that it -- you know, it can't be a packet, then you're reading out 4A, which shows by their own definition a group of 1s and 0s. So we think that's another inconsistency in their argument, Your Honor.

And finally, Your Honor, just on the -- I address this briefly, but on the address of either a row or column on memory locations, there wasn't a lot of dispute I don't think on that in the briefing in terms of what type of information. It's all about what a signal is. That's really what the debate is. I don't think there's much debate on this.

With that, Your Honor, unless you have any questions, I'll turn over.

THE COURT: Nothing further. Thank you.

Let me hear from Netlist, please.

MR. SHEASBY: Your Honor, there will be presented in this case system art that involves the use of packetized transfer of data, just as there is written prior art in the PTAB that involves the transfer of packetized written data. So the issue is live for validity but it's validity that's going to happen in this court, not just validity that's going to happen at the PTAB because they're going to present the mirror image system art before Your Honor.

I can do this relatively quickly. So the -- historically there was never a debate about whether packetized information was a signal or not. That wasn't live in the issue that was before in the Northern District of California in *Google*. There is now a live debate as to whether packetized information constitutes a signal.

And Madam Courtroom Deputy, if I can have the elmo.

We know that the issues are not the same because this is the language that was proposed in Google of 'varying electrical impulse that conveys information from one point to another'. That was the Google proposal. You will notice that that is not the proposal of either Micron or Netlist, and there's a reason for that. It's because they want to say we've disclaimed something and then alter it to make it more possible for them to argue that packetized information constitutes a signal.

A -- packetized information --

If we go back now.

Packetized information and a signal are different things. The courtroom -- the --

May I approach counsel's bench, Your Honor?

THE COURT: You may.

MR. SHEASBY: Thank you, Your Honor.

Counsel's table.

The issue is -- and this is the embedded issue. So there's -- sometimes people say plain and ordinary meaning because they want to avoid a debate. Plaintiffs do that too often and it's not, I think, appropriate. This is not a situation in which we want to avoid debate; we want to engage forthrightly with a debate, which is we don't think they should be able to argue that 'packet' equals a 'signal'. And going from 'packet' to the Northern District of California construction and then changing the Northern District of California construction to some arbitrary additional language that they've added in is all in the stead of one thing, of saying a signal is a same as an encoded data of packet. Mr. Holbrook, who's their corporate representative, testifies that it is not.

The evidence that a signal is not an encoded packet of data comes directly from Figure 4A and Figure 4B that my brother showed, and I'll explain why. D0, D1, D2, D3, those are defined in the specification as signals. Each of them is

a separate signal. That's the whole point. They're trying to say that altogether is a signal. That's not a signal in the specification. Mr. Holbrook on slide 49 makes clear that the signal is different from a packet. And all they're doing through this claim construction is nudging, nudging, nudging closer to this argument that a signal is a same as a packet. That's a packet altogether when it's encoded, but we -- each of those is defined separately as a signal, Your Honor. That's all I need to say.

THE COURT: All right.

MR. McKEON: Your Honor, may I make one quick point?

THE COURT: You may.

MR. McKEON: I just want to clarify. The definition of 'signal' that we propose in this case is exactly the same definition that Netlist agreed to previously. There's no distinction. The only difference we had was 'row/column address signal', which is a different term. We took the definition of 'signal' that Netlist agreed to and added the row and column memory locations, but that's the only thing that's different. Thank you.

THE COURT: All right.

MR. McKEON: Thank you, Your Honor.

THE COURT: Let's move on to the 'logic element generates' from the '912 Patent. And Plaintiff proposes plain and ordinary meaning and then there are a set of discreet

definitions proposed by Defendants.

Let me hear from Plaintiff on this first.

MR. SHEASBY: Slide 53, Ms. Truelove.

THE COURT: Tell me why the Defendants are wrong here.

MR. SHEASBY: Sure. So the whole game is replacing the phrase 'received by' with 'used', and so it's just a pure exercise in claim redrafting. The basis for that exercise in claim redrafting is the CRU proceeding as well as the PTAB and the Federal Circuit affirmance of the validity of the '912 Patent. And what we talked about in that context was that Amidi, which was the prior art reference, did not send all -- did not -- not all four signals were received by Amidi. This was on slide 55. And because of that, we distinguished that our system was different because we responded to the receipt of all four signals.

We did not use the word 'use' to apply to all four signals on page 55 -- page 56. There is a reference to 'use'. There are two references to use in our appellate brief. One is not requiring use of all four signals and one is requiring just a basis -- a reference to the specification, not for the claims.

So there clearly was an attempt to disclaim -- to sort of claim around prior art, and that happened by saying 'in response to all of these four signals' and specifically

listing all the four signals. That's the claim language itself. The redrafting of response to use is just an attempt to create additional ambiguity, because then once we get to 'use', there is going to be debate about what does it mean to use all four signals.

So, for example, in the specification -- if you go to slide 54, it describes receiving all four signals, including a bank address signal, a row address signal, a column address signal, et cetera. But in some situations it may not send all of those four signals onto the memory device.

So this is, once again, trying to -- it's trying to avoid a subsequent debate which, is what we're going to have in front of the jury, is about what 'use' means. And the claims say in response to the argument in front of the Central Reexamination Unit and the federal -- and the PTAB was about the fact that our claims say 'in response to'. There are two references to 'use', but neither of those references relate to all four of the signals that are recited in the claims nor to the claims themselves.

And so I think going from 'in received to' -- 'in response to' to 'use' is just claim redrafting.

Thank you, Your Honor.

THE COURT: But didn't Netlist amend these claims during re-exam to require that the logic element generates specified output signals in response to all four enumerated

signals?

MR. SHEASBY: Absolutely. And we are bound by that and we live with that. The problem is the embedded dispute is that what they want to do is convert -- and this is -- on slide 53, the issue is they want to convert 'in response to' -- 'receive and act in response to' to 'used'. They're trying to redraft the claim language.

We are bound -- so let me give you an example. That claim language was added. There's no equivalence available on that claim language--right?--except if you go through the steps that would a avoid -- you know, there's certain circumstances. But there is -- there was prosecution disclaimer based on the amendment of the claim by adding that limitation. There's no doubt about that. But that doesn't mean you get to go from the language in the claim and re-alter it to use the word 'use' because of two passing references to 'use' in the Federal Circuit briefing, which is what they're trying to do.

THE COURT: All right. Let me hear from Defendants, please.

MR. DRYER: Thank you, Your Honor.

THE COURT: Good afternoon, Mr. Dryer.

Please proceed.

MR. DRYER: With all due respect to my friend on the other side, I think it's really Netlist that's trying to

redraft this claim and not Defendants. As you can see here on slide 67, the proposed construction does not use the word 'use', which my friend was so concerned about. It uses 'in response to'. What Netlist wants to say, though, is you don't actually have to use the signals in any way; you can just receive them; you don't have to use them as long as you receive them. So they're trying to replace 'response' with 'receive'.

I think, respectfully, you can't generate output signals based on all four input signals without using all four input signals. So to that extent there is a disagreement about 'use'. But that's not what the construction that we've proposed says. The focus of our construction is clarifying that all four of the signals need to be used even though some of the claims, not all of them, but some of them recite at least in part. And that 'at least in part' could create an ambiguity that the jury, without a construction, might think 'in part' means--I can use three of them but not the other one or can respond to three of them but not the other one. That can't be right, and we know that from the disclaimer, which I think Mr. Sheasby agreed occurred during the re-examination.

The amendment itself, of course, uses the conjunctive 'and' to group these signals together. So that alone -- I think the plain reading of that would be that all four have to be responded to or used.

Then Netlist, you know, distinguished the prior art on that very basis. And then they doubled down on it on an appeal to the Federal Circuit saying that it has to respond to all four enumerated signals. In fact, they even characterized themselves as having made a disclaimer when they went up to the Federal Circuit.

Here you can see the amendment on slide 69. I think, again, the language kind of speaks for itself. Here's -- on slide 70 and 71 you have the argument that they made, and I think it's very important here, the key point is they say that Amidi CPLD 604 never receives bank address signals, that's one of the four enumerated signals; therefore, the control signals can't be generated based on bank address signals. So it's talking about generating the signals based on all four inputs. And because Amidi was missing one of those four inputs, it wasn't generating its output signals based on all four.

On the Federal Circuit, again, they reiterated this point very strongly. They said they unequivocally disclaimed any broader meaning. And, you know, as concerned as they are over the meaning of 'use' now, they didn't have any problem understanding what it meant in their own Federal Circuit brief because they used the word 'use' multiple times. And respectfully, I think, if you actually read the context in which they used the word 'use', it's not as narrow as they claim in their reply brief.

With respect to page 28 of Exhibit Q, here, yes, it's true that they only mention using two of the signals here, but if we're construing 'response', if that's what we're doing, if 'response' means you have to use those two, then there's no reason it would mean only those two; it would be all four, because that's what -- the claim language is consistent for all four.

And then with respect to Doctor Sechen's declaration that they referred to on page 34 of their appeal brief, this is where Doctor Sechen was offering an opinion, the specification provided a written description to support this new limitation. And in doing that, he said the specification teaches using all four. So if you need to use all four to have a written description, then that must be what you're trying to add.

And, finally, they point out that there is embodiments where certain of these signals aren't used. We haven't disputed that. But when you narrow your claims in re-examination, it's only natural that you're going to be narrowing them in a way that excludes some of the disclosed embodiments, and that's what the Federal Circuit recognized in the *Plastipak* case. And so the fact that, you know, applying this disclaimer might exclude certain embodiments is not controlling here.

Unless Your Honor has any questions.

THE COURT: No. I think I understand your

arguments.

MR. DRYER: Thank you.

THE COURT: Anything further, Mr. Sheasby.

MR. SHEASBY: No, Your Honor. Because of time, I'll move on.

THE COURT: All right. Let's move 'a memory module connectable' 'a memory module operable' from the '912 and '608

The issue here seems to be whether the preamble is or is not limiting.

I'll hear from Netlist first.

MR. SHEASBY: May it please the Court. I can do this claim by claim.

So the first dispute relates to the '912 Patent. It refers to 'a memory module connectable to a computer system'. 'A computer system' provides antecedent basis to the reference to input signals received from the computer system. And so if you didn't have a memory module connectable to a computer system, the idea of the computer system sending signals that are received by the memory module would lack antecedent basis and, therefore, be indefinite. That's slide 62, claims 15 of the '912 Patent.

Slide 63 is claim 1 of the '608 Patent. It refers to 'a memory module operable to communicate with a memory module via a memory bus', and that memory bus has certain signal lines, and that -- a memory bus and a set of control address signal

lines, the indefinite article provides antecedent basis for the reference to the memory bus and the set of control address signals in the claim itself.

So, once again, the preamble is limiting because it provides antecedent basis for the source of those memory bus and control address signals.

Thank you, Your Honor.

THE COURT: Let me ask you this before you sit down. The Defendants in their briefing argue that what led the Court to find the preamble's limiting in *Samsung* 1, we'll call it, are not present here. Do you agree with that or disagree with that?

MR. SHEASBY: No. Actually I think the -- it was a closer case in *Samsung* 1. In *Samsung* 1 there was one -- there are two reasons why the preamble is limiting. One, if it provides antecedent basis, or two, if it gives life and meaning to the claim as a whole. Judge Payne found that the preamble was limiting in the *Samsung* 1 case based on the life-and-meaning analysis. You don't even have to get to the life-and-meaning analysis. This is black letter law that antecedent basis requires the preamble to be limiting.

THE COURT: All right. Well, I'm not sure that there was an answer to my question in there or not. I take it you're telling me that this is a different situation --

MR. SHEASBY: This is a different situation, yeah.

I don't think you can read Judge Payne's decision and say that leads me one way or the other. In other words, Judge Payne thought a memory module was important because otherwise the limitations could read on random things put in graphics processing units or computers themselves, and on that basis he felt the specification required him to find 'memory module' limiting. All that exists here, but that's sort of the tail wagging the dog. The dog here is the antecedent basis, which the Federal Circuit requires.

I'm sorry for not being fully responsive the first time, Your Honor.

THE COURT: All right. Thank you.

Let me hear from Defendants.

What's your position, Mr. Dryer?

MR. DRYER: First I'd like to start with a small procedural point, Your Honor. The antecedent basis argument that my friend on the other side just made actually doesn't even appear in their opening brief. Their opening brief relied exclusively on the life-and-meaning prong of the analysis, and it was only in their reply that they brought up these two antecedent basis arguments. So I think the Court would be well within its discretion to disregard them.

On the merits, the life-and-meaning, I think they haven't made the showing in this case. First of all, they haven't shown that the factors that led Judge Payne to find in

Samsung 1 that the preamble was limiting, they haven't shown that to be the case here and they haven't shown why the -- you know, they haven't explained, for instance, how these claims could hypothetically read on a graphics processor or some other type of component, which was the concern that led Judge Payne to rule the way he did.

And on the merits of the antecedent basis issue, I think it's really -- it's redundant if you read, say, 'a computer system' in the '912 Patent as limiting in the preamble because the body of the claim requires a computer system to be providing signals.

So I think if you are just going to take 'computer system' and say that part of the preamble is limiting because it provides antecedent basis, then it would not be changing the scope of the claim in any way. It's kind of a non-issue really. It's a redundancy. And the same is true for the antecedent basis argument they make for the '608 Patent.

THE COURT: All right.

MR. DRYER: But in either case the law is clear, even if one piece of the preamble needs to be construed as limiting, it doesn't convert the entire rest of the preamble to limit it.

Unless you have questions.

THE COURT: No, sir. Thank you.

Okay. Let's move onto the data buffer terms.

And let me hear from the Defendants first.

Again, Plaintiffs are proposing plain and ordinary meaning, but Defendants have discreet constructions they've offered up.

DR. ALBERT: Thank you, Your Honor. Frank Albert for Samsung.

May I proceed?

THE COURT: Yes, you may, Mr. Albert. Doctor Albert, I should say.

DR. ALBERT: Thank you, Your Honor.

Your Honor, the dispute here regarding the what we call the buffer control terms is a dispute that was before this Court in *Netlist* 1, and the question is whether these terms -- these are very long, very complicated, but these terms as a whole require there to be a so-called fork in the road. And here what we're talking about is not the inside of the buffer, but whether there is a signal input and that data goes to one of two outputs.

THE COURT: In other words, when data is being transmitted to one device, does that automatically mean that the other devices are somehow electronically isolated.

DR. ALBERT: That's the exact dispute, Your Honor.

THE COURT: Yeah. So tell me why your side of the dispute is the right one.

DR. ALBERT: Thank you, Your Honor.

So you may be asking yourself, Your Honor, why we have the same dispute for a different patent in another case. And if you look at the patents, the '215 and '417, for example, they share an inventor with the '339 that had this dispute in *Netlist* 1. Both patents -- sets of patents are directed to buffers. They're both from around the same general time from the same company. Kind of makes sense that the shared inventor had a similar solution to a similar problem.

And in *Netlist* 1 the Court dealt with the same issue and it found that when describing a problem to be solved, the patent emphasized reducing load at the outputs of the memory devices. And in addition, the Court went on to say that the sole embodiment describing path selection during a write operation disables one path within the buffers and the other path is enabled. We have a very similar situation here with these patents, the '215 and '417.

So starting with the --

THE COURT: Isn't your position, at the end of the day, really based on some theory of disclaimer? I mean, you don't really call it that in your briefing, but isn't that really what this is?

DR. ALBERT: That is certainly one aspect of why this Court should hold for the fork in the road. It starts with the claims, it goes to the specification, we talk about the problem to be solved, and the solution. This is the

solution. This is the only solution that is described. And then that's why during the appellate procedure for the prosecution history they described a key aspect of this invention was essentially to have this fork in the road. They called it selective enabling. And I'll get to that in a bit.

So; I wouldn't necessarily only rely on disclaimer, but that is certainly a part of it. That is certainly something that pushes it along. But if you look at the totality of the evidence, Your Honor, we think each step along the way shows that there's a fork in the road, starting with the claims, going to the specification, then going to the disclaimer. And we do cite specific disclaimer law in our opposition brief.

THE COURT: Are the claims at issue here clearly directed to load isolation?

DR. ALBERT: We think they are, Your Honor. So if you go to, for example, claim 2--sorry--'215, claim 1, Netlist, as you've seen from *Netlist* 1, they are, you know -- they're kind of masters at creating these very long claims. Some of these claims go on for a page, a whole column, column and a half. Some of these limitations are full paragraphs. Here is one such example. And here what we're talking about is it's this logic coupled with the buffer and it's for providing control signals to the buffer to enable communication.

And what is it actually doing? If you read the claim,

you've got a first set of logic signals that enable the communication to one device and then another set of signals that enable the communication to that other device. And it's that combination, as recited in the claims themselves, of enabling one and then enabling the other, these different devices, is what creates that fork in the road.

And here we have a very similar approach for claim 21 of the '215. It's that creating, that enabling of that first device, and then with something different doing that enabling of that second device.

A little bit different -- excuse me. I skipped to a slide for the '417. It's very similar language. And here it's instead of the, you know, 'enabling', it's 'circuitry being configured to transfer the bursts'. And here it's in the one of the plurality of N-bit wide ranks. And so it's actually talking about taking the multiple ranks and only triggering the bursts of the data from one.

And so how is that actually described and how does this come about from the specification? The specification talks about this problem of too much load. When you take a system -- prior art systems where you have one, two, three, four devices, and you wanted to make a device -- a module with more devices, more memory, what that is going to do is it's going to stack up that load; it's going to increase the load on the system. And what they say here in the background of the

invention is that things like that are things that reduce the capabilities, that reduce your design. And so this -- these challenges are preventing you from creating these modules with more capacity.

And then it describes in the patent this conventional memory module. And here we have Figure 2 of the '215 and '417 Patents, and what I've circled here in red is the memory devices 30a and 30b. And you see the output of each memory device goes to a common line. And what they're saying is that when you electrically couple the memory controller computer system, the load of both memory devices is exposed to the computer system. So without some intervention, as you increase the number of devices, you increase the load.

And then the patent, the very first thing it says in the detailed description about how to solve that problem was load isolation. And here what the patent describes is the selective isolation of one or more of the loads. So you take the module that has now too much load for the system and you disable some of the devices. That is the fork of the road. You disable some of the devices to reduce the load. So here on the right, "The load isolation advantage allows the memory module to present a reduced load." And how does it do that? I've got it underlined--"selectively switching between the two ranks of memory devices."

And then it goes on in that very same section, using

this feature allows you -- it says may -- it allows certain embodiments in which the loads of the memory module may otherwise limit the number of ranks. So by having this switching, this solution, it allows you to have, according to Netlist in this patent, more memory. This was the solution that was directed at the identified problem that provides that enabling of one memory device in the claims and then the enabling of the other memory device.

THE COURT: Where is this actually called out in the claim language? For example, take claim 1 of the '215. Where is the claim language that supports this fork in the road concept?

DR. ALBERT: So we say that it's in the entire language where it talks about providing the first control signals to the buffer to enable -- first enable communication of the first data burst. Right? So you have one signal that enables the first data burst between the first memory integrated circuit and the memory controller. That's the first set of devices where the switch is turned on.

And then you go on in claim 1 and it talks about where the logic is further configured to respond to the second memory command by providing a second control signal to the buffer to enable communications of the second data burst between the second integrated circuit and the memory controller. That's when the switch to the other memory

devices are turned on.

Thank you for that question, Your Honor. We looked to this claim language and we had a similar question. We read the specification and we asked ourselves how did this claim match up with the specification. And if you look at it as a whole and enabling one and enabling the other, that's how it matches up with the specification.

THE COURT: And that's how you get to the fork in the road.

DR. ALBERT: That's how you get to the fork in the road based on the plain language of the claims.

THE COURT: Over.

DR. ALBERT: However, the specification, again, talks again about the load isolation as being the solution to the identified problem. And then if you go to the figures, each figure that talks about presenting this data, routing the data through this buffer, which is required in the claims, every embodiment that talks about routing that data through a buffer, sometimes called a switch, but a buffer or switch, it's doing so with this fork in the road.

So here is a description of Figure 4A, and what I've highlighted here is the fork in the road. The blue is the input line to the switches and the red is the output line out of those switches. And so you have the two inputs and the one output, you have that fork, and that's exactly what the

specification describes for this figure. It talks about selectively allowing one of the first DQ data signals lines from the DQ data signal line 102a compared to 102b. So it's talking about that selectively allowing that data to go through.

And so what I've shown here on slide 89, Your Honor, is those two different paths, the two different tines of the fork, if you will, where you can receive data from the devices 32a on the left are received data from the devices 32b shown on the right.

If look to the other figures of the patent, Your Honor, it's consistent. There's some -- there is a dispute about whether there is an embodiment that does describe something that's not a fork in the road--I'll get to that later--but if you go to the figures of the patent, each of them that talk about the data going through the buffer, talks about this load isolation solution of having that fork in the road. Here I've got 3a on the left, 5a in the middle, 8c on the right; they all have that two tines on the left, one tine of the fork on the right.

Now, one other aspect of these claims, Your Honor, is not just the switches or the buffer, but it's how those switches are controlled. That's -- if you go back to the claim language, it talks about control signals that control that buffer. There's only one place in the actual body of the

specification that talks about those signals, and what it's doing there -- what those signals are doing is enabling and controlling that fork in the road. So here I've got the two examples on the left, the actual quotes, and the Figure 5a that it's describing on the right, and yellow on the right is the highlighting for those signals.

So we got the switches in green on the right and we got the logic elements up at the top, and then the signals are the signals that enable and control that selective isolation by those switches. It's the only description in the body of the patent regarding that control.

Now, getting to your disclaimer question, Your Honor, you asked whether it really is an issue of disclaimer. Again, we think from the plain language of the claims as well as the description and, you know, how the patent distinguished the conventional systems in the patent itself, disclaimer is not necessary, but if the Court decides to go there, into disclaimer, disclaimer absolutely carries us forward and limits this invention to only a fork in the road; the selective isolation, if you will.

So here I have on slide 95 is Netlist's description in the appeal brief for a related patent. And, you know, I'd like to address front, Your Honor, in the opening brief Netlist had kind of a buried statement that, you know, none of our evidence of other proceedings is even relevant because

there is different claim language. And in our responsive brief we put in case law that says exactly why this is relevant.

If you have a disclaimer or -- you're not just talking about particular claim language of a parent, but if you're talking about the invention generally, then that prosecution history applies through that entire chain even if you have different claim language. So we put that in multiple cases in the brief, in our response, and in the reply brief we didn't see a response to that; we didn't see a response why that was wrong.

So going back to that disclaimer, let's see the actual merits of how it affects the case. So here we have Netlist's description of that same figure that I presented earlier. Netlist described that that figure can selectively electrically couple each pair of data lines--same description as I presented earlier.

And what did Netlist say to the Federal Circuit? Netlist said that the configurability to selectively electrically couple a device data line to a common data line was a key contribution of the inventions; not a key contribution of some specific claim language, but a key contribution of the inventions.

Now, Netlist is saying that, no, there is no requirements of selectively electrically coupling in this -- these

particular claims, but what they said to the Federal Circuit for a related patent was that that exact requirement was a key contribution of the invention. And they went on to say, When a switch or other mechanism is used to selectively electrically couple the data lines, such as Figure 3A--I showed that earlier--the electrical load of the memory devices can be disconnected from the computer switch.

THE COURT: So when they say that to the PTAB in a proceeding with a different, although albeit related patent, that somehow rises to the level of disclaimer even though that language is not in these claims.

DR. ALBERT: Exactly, Your Honor.

THE COURT: Is that your view?

DOCTOR ALBERT: That's not just our view, Your Honor; that's the Federal Circuit's view. We cited three cases in our responsive brief. Netlist did not respond to those three cases.

THE COURT: All right. What else, Doctor Albert?

DR. ALBERT: There is -- that -- we're not just dialing with an isolated statement to the Federal Circuit. Again, this is not statements that we're relying on to the PTAB; it's statements to the Federal Circuit in the appeal from that PTAB proceeding.

And they go on to say, "Solving the problem of increasing load due to additional memory devices was essential to

overcoming the shortcomings of the prior art memory modules." And remember, the solution that this patent described for the load isolation problem was the fork in the road.

Then it goes -- then Netlist went on to say, "The inventor solved these problems by designing logic and circuit elements to perform memory density multiplication and to selectively electrically couple and load isolate individual or groups of memory devices, thus avoiding the increased electrical load of the memory devices." Again, they're talking about that fork in the road.

THE COURT: All right. What else? I'm happy to hear it if you've got something else, but we do need to move on.

DR. ALBERT: Sure.

Netlist also pointed to this Figure 8 and Figure 8B from the patent claiming that there's some sort of embodiment that envisions not having this fork in the road. We got to start with the claims, Your Honor, and the claims require that data burst going through the buffer. And if you look at Figure 8A and 8B, the data is just hard-wired, like the conventional system, hard-wired to the output. There is no switch, there is no buffer that that data is going for. So 8A and 8B just don't apply to these claims.

Then, finally, Your Honor--it's my last slide, I believe--the -- with regards to Figure 8A and 8B, the claims

also require that the control signals to the buffer, if you look at the description of Figure 8A and 8B, there's no description of that control signal; you have to go back to Figure 5, which I showed the fork in the road.

One last point, Your Honor, Netlist points to a -- the -- some language in the abstract for support for the -- for an alleged broader meaning. We don't think it really supports them because it doesn't say anything that negates the rest of the patent. However, one thing that was actually very surprising to us that they're relying on the abstract, because the abstract to this invention was added in 2017. They're claiming in their infringement contentions that the priority date is 2004. So if the invention is to be interpreted as of the date of the invention, say it's 2004, then the abstract can't change that meaning. And if it can change the meaning, we've got a problem, because if 2017 is now their allegation of what the priority date is, which is in conflict with their infringement contentions, then they're accusing the prior art of infringement in this case and this case should be over.

Thank you, Your Honor.

THE COURT: All right. Let me hear from Netlist, please.

MR. SHEASBY: Your Honor, I'm having a technical difficulty.

THE COURT: That's fine. Take a moment to see if

you can work it out.

Let's go off the record while he does that.

(Pause in proceedings.)

THE COURT: We're back on the record.

Go ahead, Mr. Sheasby.

MR. SHEASBY: Thank you for your indulgence, Your Honor.

I think there's a lot of what Doctor Albert said that is right, but I think that he -- his ship sort of crashes on two shoals. The first is that there is a concept in the Federal Circuit where -- in which -- Your Honor, I need to make one more brief adjustment.

THE COURT: That's fine.

MR. SHEASBY: The -- if I could have slide 79, Ms. Truelove. Thank you.

There is a concept in which a disclaimer in a parent can apply to a child, and the -- and it doesn't necessarily turn on any one particular claim term, but it turns on the claim itself that was the subject of disclaimer in relationship to the claims that are at issue in this case. And where the disclaimer argument fails is it's not an accident that they didn't show you the claims from that unrelated -- or that parent application and explained why those claims are the same or substantially the same or related, not just based on one word but even conceptually the same as the patents in this

case.

There is a load isolation embodiment in the specification--I'm on slide 80--and we actually have patents that have been issued on that load isolation concept. This is the '774 Patent. The '215 Patent and the '417 Patent don't recite load isolation. They also don't recite the drive concept that is in the '339 Patent that was the subject of the -- Judge Payne's ruling on the '339 Patent. And the concept that the -- there is no language in the claims that references the isolation. There's no language in the claims that talks about selectively switching. The language in the claims talks about the fact that there needs to be an independent path for both -- for buffers to -- for control signals to two separate ranks. It doesn't say that they are isolated or selectively turned off.

I should also point out, the issue is the presence of a switch that cuts off one and cuts off the other. And the argument, which was a new argument made for the first time that there's no buffering on the DQ line, box 40 is the buffer, and you'll see that in Figure 8a the DQA, which is the data line, goes through the buffer, so it's buffered but it doesn't have the switches that are necessary to create the selective isolation.

So Figure 8A is an example of both a data line that's buffered and also a data -- and also a data line that doesn't

have a switch that isolates each one of them separately.

So I think that Doctor Albert has, respectfully, misinterpreted claim 8A, and I think he falls on a basic fact that 'isolate selectively' or those concepts are not in the specification -- are not in the claims. The claims are directed to a different portion of the specification.

THE COURT: You mean Figure 8A, not claim 8A.

MR. SHEASBY: Figure 8A, excuse me. And I think the claims are directed to a different portion than the selection isolation portion of the specification.

Thank you, Your Honor.

THE COURT: Okay. All right. Let's move onto the 'logic' term, which I understand is contested by Micron only and not Samsung. Micron's position is that this is subject to § 112, ¶ 6 and is indefinite; plaintiff's position is that it's not § 112, ¶ 6 and should be given its plain and ordinary meaning.

Let me hear from Micron first on this.

MR. RUECKHEIM: If we can have -- Your Honor, Mike Rueckheim on behalf of Micron, and I will try to make this very quick.

THE COURT: Please proceed. Obviously we don't have 'means for' here, so we don't have the magic language to open the door to § 112, ¶ 6.

MR. RUECKHEIM: We do not. What we have is the word

'logic', which the Federal Circuit has recently found in the *Engenera* case to be a means-plus-function term. We had the 'configured to' that's shown on the slide in green. And 'configured to' has been found in many cases, *MTD Products* identified in our briefing, to be one of these transition terms like 'means for'. And then we have in blue the function language from the top of the screen is the '215 Patent, the bottom is the '415.

And so the *Engenera* case says that it may be 'circuity', it may be 'logic', and *Engenera* dealt with the term 'logic' 'logic to modify'. Maybe there's some structure there, but you have to have sufficient structure for the actual functions identified or known to one of skill in the art in the context. And so what we did was we asked our expert, the only expert who opined on this issue, is there sufficient structure here, and he said no. He said the logic here can relate to any kind of hardware, software, or what have you.

What Netlist points to in its opposition brief or in its responsive brief is that there are statements in the claims that recites the logic is coupled to a buffer or the logic is coupled to a printed circuit board. *MTD Products* looked at this 'coupling' type language, *Engenera* cited in the brief as well looked at this 'coupled to' type language and found it was not sufficient unless you can identify some type of structure for the inputs and outputs that would inform one of

skill what the logic is referring to here.

I think this case is a unique case for the term 'logic'. I have the entirety of claim 1 of the '415 Patent--it's long--on the screen, and you'll notice that it has two words in it--'logic' and 'circuitry'. And we're resting on the briefing for 'circuitry', but I do think it's interesting that we have these two words in here that are presumed under the law to have different meanings and Netlist has not indicated at all what it believes these meanings are. Micron believes both of these terms are indefinite.

Once you find -- that the Court finds this term is means-plus-function, we asked our expert to look at the specification and see if there's any structure to support that it's tied to -- that it's clearly tied to the function here; the expert said no.

Netlist in its briefing did a string cite of a number of different pages in the specification. This is from their reply brief on the slide. They point to in the bottom of the screen this logic -- there is some disclosure in the spec of a logic element that's configured to receive control signals. But what the Court needs to do is see if there's structure that's tied to the function of the claims. That's all the blue language on the slide. It has to receive these control signals--that's the '215 Patent; it has to respond by producing different control signals. The '415 involves

control signals, address signals, and it also discusses it being further configurable to help put data buffer signals, and there's been absolutely no showing of anything in the specification that meets this language.

Unless there's any questions.

THE COURT: No, sir. Thank you.

Let me hear from the Plaintiff in response.

MR. SHEASBY: I think my brother -- this is Jason Sheasby for Plaintiffs.

I think my brother pointed out there was a Federal Circuit case that talks about 'logic'. That case is a situation in which the claims could read on software. These claims are not software claims; these claims are about memory modules with physical structures. Those physical structures, logic, have input and output. On slide 67 and 68, those input and output are expressly described. And the concept of logic is not a concept that could be anything other than hardware in the specification.

On slide 72, '215 Patent, column 6:36 through 48, the logic element is expressly described as a circuitry, a physical circuitry. This is the circuitry that is described as performing the functions in the claims themselves.

Doctor Stone seems to have had a change of heart between his declaration and his specification -- and his deposition. In his deposition, the first thing he admits is that the term

'logic' is a structure of circuits, and this is in his discussion of -- you can't see it from this passage, but this is from his discussion of the logic issue.

And when we asked him --

THE COURT: I don't see the word 'logic' there anywhere.

MR. SHEASBY: I know. It's not there. I haven't captured the same thing, so you're not going be able to rely on that without more context, Your Honor.

This is Doctor Stone talking about logic, and that logic is -- has gates, and they're sometimes referred to as transistors, and those transistors have specific structure. This is on slide 75. He was asked that logic includes circuitry with state and circuitry without state. His answer was yes. He said those are actual structures that you can go to a textbook and look up. In other words, he's able to look at circuitry and determine whether that circuitry is logic, which is what the claim requires. This is on slide 77. One again, he can look at logic and determine what that structure requires.

And so what we have is a couple of points. There may be some patents in which logic could theoretically be software or something else and there could be nonce, but in this patent logic is circuitry. Logic circuitry is a physical structure that Doctor Stone admits he can go and find and determine

whether something is or is not logic circuitry. That defeats the indefiniteness claim because he can actually look at a circuitry and say is this or is this not logic, as defined by the claims. And, of course, the specification provides detailed descriptions of structures that can be used to perform the exact functions on 78.

So putting aside the fact that I captured the wrong portion of the Doctor Stone's declaration in my slide, I think it's very clear from his deposition testimony that logic is structure, he can go and define that structure, look at it and determine whether that structure satisfies the definition of logic. And in these claims, the input and the output are both defined as to what the logic does, which moves them outside of that Federal Circuit case.

Thank you, Your Honor.

THE COURT: I hear your argument on structure, structure, structure, but what about the issue of whether this is or is not subject to § 112, ¶ 6? If it is, then we get to whether or not there is structure to determine whether it's definite or not, but you never did really tell me whether you believe this is or isn't § 112, ¶ 6.

MR. SHEASBY: It's not § 112, ¶ 6, and the reason being in this context 'logic' is not a nonce term; 'logic' is a circuit. And Doctor Stone admitted that 'logic' is a circuit. That circuit can be looked at and defined and

determined if it satisfies the definition of 'logic'. And in this case 'logic' is defined as having a particular input and producing a particular output, so it's describing a very particular type of logic circuitry, Your Honor.

THE COURT: All right.

MR. SHEASBY: Thank you, Your Honor.

THE COURT: Thank you, Mr. Sheasby.

Anything else, Mr. Rueckheim, before we move on?

MR. RUECKHEIM: Quickly, Your Honor.

I just wanted to point out, Mr. Sheasby pointed to a couple of statements in the specification regarding 'logic'. He didn't argue that these statements, the PLD, or what have you, are in any way limiting to the claim. He didn't argue that these PLD and the other sections he pointed to with respect to 'logic' were somehow enabled to do the functions at all or described to do the functions that are recited in the claim. He didn't point out the fact that there's other references to 'logic' like logic translation equations being programmed into various components as well in the specification.

I'll just also throw in that Doctor Stone did not have a change of heart. Doctor Stone was not asked whether he believed the circuit in the context of the claim means the same thing as 'logic', which would be against the presumption that these two claim terms used in the same claim had

different meanings. He was asked generally about logic with gates, he was asked logic about computer logic. Mr. Sheasby showed a picture of a question about a series of circuits. He wasn't asked about the context of this patent.

The Federal Circuit said in general, outside the context of any specific patent, this term can be means-plus-function. In the context of this patent, it is a means-plus-function term because there is no specifying term in front of 'logic', there is no description in the specification that would limit the functions being referred to any structure.

Thank you, Your Honor.

THE COURT: All right. Thank you.

All right. Per the parties' agreement, I'll take the term 'circuitry' under advisement and rule on the briefing there without oral argument.

We're going to move onto the remainder of the terms, although I want to remind counsel that if we run out of time before we hear -- the Court hears argument on some of these remaining terms, I will also simply determine what the proper claim construction should be based on the briefing.

All right. Let's move on to 'at least one of the circuit components' from the '215 Patent. This, again, is a dispute between Plaintiff and Micron only. Micron says it's indefinite; plaintiff says plain and ordinary meaning. And I think the dispute is probably whether or not there is or isn't

a lack of antecedent basis.

But let me hear Micron's argument first.

MR. RUECKHEIM: Thank you, Your Honor.

Your Honor, I have one slide for you. Claim 14 is potentially the antecedent basis. The term that we're dealing with is in claim 15. Claim 14 recites a buffer that includes circuit components. Claim 15 has the language that's the problem, the 'at least one of the circuit components'. And so there is no antecedent basis.

Netlist argues that the Court can construe this term, can fix this term. The problem is there's no support one way or the other as to what this term means. Is it reciting that there is one circuit component that does both the functions in claim 15, provide the first path in response to one signal and provide a second path in response to the second control signals, or is it saying that all the circuit components that are recited in claim 14 are configured to do these two functions, or both. We don't know. We think the term's indefinite.

Thank you, Your Honor.

THE COURT: All right. Let me hear from Plaintiff, please.

MR. SHEASBY: If I can have slide 100, Ms. Truelove.

THE COURT: Now, if he just had one slide, you only get one slide.

MR. SHEASBY: Your Honor, I will just use one slide.

THE COURT: All right.

MR. SHEASBY: So I think what my brother is confusing is that a claim is breadth versus indefiniteness. So the only question for indefiniteness is whether there is antecedent basis for these circuit components, and there is antecedent basis because the claim before it refers to circuit components. Everything else he said about, We don't know if it can be one or both, the breadth of the claims doesn't make it indefinite; the only indefiniteness argument is that is there antecedent basis for the circuit components. There is. It's the components that are within the buffer. So we know what circuits to look at to examine where the claim limitations are met.

All this other stuff that he's talking about goes to the question of proof of infringement, not whether you don't know what circuit to look at. We know what circuit to look at it. It's the circuits in the buffer.

Thank you, Your Honor.

THE COURT: All right. Anything further from Micron?

MR. RUECKHEIM: Nothing further, Your Honor.

THE COURT: Okay.

Let's go on to 'burst of data strobe signals' from the '215 as well. Similar situation--Micron, the opposing party

to Plaintiff, is arguing indefinite; plaintiff's saying plain and ordinary meaning.

Let me hear from Micron.

MR. RUECKHEIM: Thank you, Your Honor.

Your Honor, the term is 'burst of data strobe signals'. The claim recites a first burst of data strobe signals, second burst of data strobe signals, and then a buffer that's configured to prevent the first burst and second burst of signals from colliding with each other.

And we asked our expert Doctor Stone, the only expert who opined in this case, what this term means, and he said, Well, it depends; it can mean a couple of different distinct things. One, it can be a set of consecutively transmitted strobe signals from at least two different memory devices. It can also mean a set of consecutively transmitted strobe signals from one single memory device. And we asked him, Well, what does it mean in this patent, and he says, Well, it doesn't say. So the claim says something that can be read in two different ways. The patent doesn't say which way you should read it.

Netlist in it's briefing said -- well, they agreed with us. That should be the end of the story--they agreed this term has two different meanings--but Netlist says the Court should interpret the term to encompass both. The problem with that is that there's two distinct plausible meanings here, and

Netlist is saying you should construe them as accompanying both, but what you need to do is look at the specification. What does the specifications say? One way or the other or combined? The specification says nothing.

This is the sole reference on the screen as to burst of data strobe signals. It doesn't say one way or the other whether these signals should be combined, whether it should be coming from one device or two. And the differences here matter. It matters for the infringement analysis. It matters for invalidity analysis. The configurations -- the structural configurations of what's being accused are significantly different.

THE COURT: Why do we need to know where this burst of data signals comes from? Why do we need to know?

MR. RUECKHEIM: It depends -- well, it's not even just the where, Your Honor; it is what is a burst of data strobe signals. Is it something that's -- I get Your Honor's point where is it coming from. Is it something coming from one rank and something coming from two, and we're trying to show that on this screen on the slide. If you look at the pink lines as your data strobe signals, at the first you see the uncombined data strobe signals coming from each device, and so basically what they're accusing, they would say the claims encompass a device that only prevents collisions from these pink lines.

If you take the second, the combined approach, you now have two different memory devices being combined on here and the strobe signal from both, and so you'd have to accuse functionality where these strobe signals from two different devices, or more, are now -- you prevent those from collision.

And so, Your Honor, just to wrap up, we think the case law here supports us; actually the *Sandoz* case. When you have different plausible meanings that yield a different result, which we've shown here, the claim can be indefinite. The other side pointed to this case *Nervo* that dealt with this -- they dealt with this issue to the extent they said the different opinions as to what the term 'configured to' means, one of the different opinions was not plausible and so they rejected that out of hand and they said, We're not going to take multiple distinctions, because in every case you could have non-plausible interpretations of what a claim term means. So we think *Nervo* is completely distinguishable and not relevant here.

Thank you, Your Honor.

THE COURT: All right. Thank you.

Let me hear from Plaintiff.

MR. SHEASBY: Jason Sheasby for the Plaintiff, Your Honor.

Two things. I was chagrined to have had a title on my slide about Doctor Stone's declaration and then had put in the

wrong portion of his declaration. For the record, the appropriate portion of his declaration where he discusses that 'logic' refers to a field effect transistor is Exhibit 5, paragraphs 38 through 39, and I apologize for the imprecision on the slide, Your Honor.

THE COURT: All right.

MR. SHEASBY: Moving on to the issue of data strobe burst and its indefiniteness, this is slide 107. Doctor Stone in his deposition was able to identify whether something was a data strobe by looking at a figure and analyzing it. And the fact that there would be different types of data strobes, data strobes that are combined versus data strobes that are not combined--this is on slide 108--doesn't make it indefinite; it means that the claims cover both non-combined data strobes and combined data strobes.

Thank you, Your Honor.

THE COURT: All right. Let's go on to 'operable in a computer system to communicate data', again from the '215 and also from '417 Patent. Both Defendants are opposed to Plaintiff here, and Defendants have offered a precise construction; plaintiff has proposed plain and ordinary meaning.

Let me start with the Defendants, and let me ask for an explanation of your proposed construction 'configured in a computer system to communicate data'.

And I'll be honest, I'm not real sure what the dispute between the parties is here, so you might clarify that for me.

MR. LIVEDALEN: Can we please adjust the --

MR. McKEON: We're getting the slides, Your Honor. Just a moment, please.

MR. LIVEDALEN: We'll just go with the slide deck. Sorry about that, Your Honor.

THE COURT: If you want to put one of your printed slides on the elmo as opposed to using the computer screen, that's fine.

MR. LIVEDALEN: That would be great. Thank you, Your Honor.

Brian Livedalen for Defendant Samsung. Good afternoon, Your Honor.

THE COURT: Please proceed.

What is the real dispute here between the parties?

MR. LIVEDALEN: Sure. So turning to slide 114 -- if you just bear with me. So the dispute here, Your Honor, is whether this term requires mere capability, including after modification, or whether it requires structure that presently is configured to perform the recited function. And so, Your Honor, if you go to our next slide 115 --

THE COURT: But the structure must be presently configured to perform the recited function. Correct?

MR. LIVEDALEN: That's correct, Your Honor. And the

issue is, Your Honor, if we actually skip to the next slide to keep this brief, this exact same issue came up in Your Honor's ruling in the *TQ Delta v. CommScope* case, and there was a latent ambiguity as to this exact same term, and we read Your Honor's decision, and in that decision there is a clarification that 'operable to' requires actual configuration to perform that function, and it's not broad enough to include mere capability, including capability that could be modified.

We did not think that this would be a term that was disputed. We offered it as part of the claim construction process, and for whatever reason Netlist has yet to agree to this term.

If we go to the next slide, in their reply brief they said, What's the big deal; there's no issue here. There was a dispute in the *TQ Delta v. CommScope* case. That dispute is not present here. And if that's the case, then Netlist should agree to Defendants' proposed construction. We've not heard any reason why they resist the construction other than them calling it vague and nebulous. But as Your Honor found in the *TQ Delta v. CommScope* case, the construction here resolved the exact latent ambiguity that exists in this case. So we ask for clarity now so the parties aren't fighting about this ambiguity later.

THE COURT: All right.

MR. LIVEDALEN: Thank you, Your Honor.

THE COURT: Thank you.

MR. SHEASBY: Ms. Truelove, could I have slide 113, please?

THE COURT: So Mr. Sheasby, is there a dispute here?

MR. SHEASBY: I think there is.

So the claims use the phrase 'operable', they don't use the phrase 'configured to', and so Federal Circuit precedent would require you to respect that separate language. I think, although I'm not so sure -- I'm not completely sure what's going on here, I think what's going on here is that in many cases these memory modules have to be provisioned by the user with sort of added information to their registers for them to perform certain functions. Certain registers must be switched on or off. And so my guess is the reason for this is that they're going to say that because there are registers that allow you to turn on and off certain features, they're not configured to -- the memory module is not configured by Samsung to do something or Micron to do something, even though it would be operable to do that if you set the particular register. And so my guess is that's what's going on here.

I read the *TQ Delta* case. It was for actually preparing for a completely different litigation. And the *TQ Delta* case cites a number of Federal Circuit opinions, and those Federal Circuit opinions deal with situations in which people had to argue that you had to break the device or use it in a way that

it was not designed to be used for, and they were arguing that satisfied the definition of 'configured' or 'capable'.

We're not talking about breaking a device here or physically altering it. My sensitivity is -- my guess is that there are registers that are -- that can be turned on and off in the memory module. They're going to argue that means it's not configured. We're going to argue it still means 'operable'. And so --

THE COURT: Have you had that discussion with the other side as to whether your supposition is correct or incorrect?

MR. SHEASBY: They have not been -- I have not spoke to them directly and said, Is this what you're planning on doing. But based on how I know these devices work, I'm at the 80 to 90 percent confidence level that this is about that registers within the device can be changed to use -- to operate in different modes, and they're going to argue that's not configured.

And so I -- for right now I would like to keep it as plain and ordinary meaning. At some point it may come up that additional construction is necessary or there's an issue to be joined. But in abstract, because of this changing in word -- this change in language, I don't think -- I don't -- it's hard for me to agree with it in abstract for that exact reason.

THE COURT: All right.

MR. SHEASBY: Clearly we can't break the device or we can't claim that if someone were to etch off a circuit it's still operable to do something, but if they're just setting a register in the device, I think that's for the jury, not for the Court.

Thank you, Your Honor.

THE COURT: Well, let me ask Defense counsel, since you two don't want to seem to talk to each other directly, let me ask you, is what he's afraid of what you're going to say? Is that going to be your position?

MR. LIVEDALEN: Your Honor, the Federal Circuit precedent is clear if there's functionality that --

THE COURT: I wasn't asking about Federal Circuit precedent. I was asking -- Plaintiff's counsel laid out what he is concerned Defendants' position will be at trial with regard to the word 'operable', and I want to know if that is a legitimate concern, or if you're telling me, No, we're not going to say that we're not going to do that, then maybe we don't have a problem here. If you're going to tell me, Yes, we are, and his supposition is right, then maybe we do. So I'm trying to get to the bottom of it. So answer the question and don't tell me what about Federal Circuit precedent says.

MR. LIVEDALEN: Yes, Your Honor.

So to the extent that there is functionality that simply needs to be turned on, we're not going to argue that that's

not operable or not configured to per Defendants' construction.

The issue in the *TQ Delta* case, which is the exact same issue here, is that the Plaintiff identified functionality in standards and alleged hypothetically that these devices could exist based on what's in the standard. In this case, Netlist is relying on, once again in its infringement contentions, technology and things that exist in the standard, not the actual device.

THE COURT: So you're not going to say because there's a register here that needs to be turned on and it's not turned on, that it's not operable.

MR. LIVEDALEN: That's right, Your Honor; the point being is that Netlist can't simply point to a standard and say the standard says that it can work with sub-devices; therefore, it satisfies all the limitations. The burden on infringement is for Netlist to show that the actual accused products are configured in the way that the claims require, and that's our position.

THE COURT: Of course, practicing the standard relates back to whether or not we're talking about standard essential patents. We've already had a discussion about that today. It hasn't been definitive, but as I said, we will get to the bottom of that issue before we get this case before a jury.

MR. LIVEDALEN: Yes, Your Honor. We appreciate that.

THE COURT: All right. Thank you, counsel.

MR. LIVEDALEN: Thank you, Your Honor.

THE COURT: Let's go to 'data buffer control signals' out of the '417 Patent.

Let me hear from the Plaintiff first. Why is plain and ordinary meaning proper here in light or in lieu of the 'selectively electrically coupled language' in the Defendants' proposed construction?

MR. SHEASBY: Your Honor, this is the same --

THE COURT: We're back to the fork in the road.

MR. SHEASBY: This is back to the fork in the road, so it's the same issue as before, Your Honor.

THE COURT: Okay.

MR. SHEASBY: I should also flag, although the -- definitively I think it's unlikely that -- unlike the '912, I can disclose to the Court I think it's unlikely that the -- we were just talking about the '417. For full disclosure, I think it's unlikely the '417 will be put forward as standard essential as opposed to infringed based on the technology, just for -- so the Court's aware of that.

THE COURT: All right. What's Defendants' position?

DR. ALBERT: Thank you, Your Honor. Frank Albert for Samsung.

THE COURT: Go ahead, Doctor Albert.

DR. ALBERT: There is substantial overlap with the fork in the road arguments from the 'buffer' terms that I argued earlier, and so I will try to limit my argument to what is not overlapping, for time --

THE COURT: Okay. That would be appreciated.

DR. ALBERT: This issue we have with 'buffer control signals', Your Honor, is that term didn't appear in the original specification. The -- that term only actually was added to the abstract summary of the invention in and around 2019, very late. But if you look to the description of the specification that actually corresponds to what they say is their priority date, it's these two quotes here on the right. This is the only description that you can even begin to say corresponds to these control signals. It doesn't actually call them 'buffer control signals', 'data buffer control signals'; it just calls them 'control signals for the buffer'.

This is that Figure 5 that I showed earlier where the -- where you had that 'logic' element at the top of the figure and that -- those control signals that would go down in yellow to the switches, and that is what was used for that selective electrical coupling. That is the only description in the patent of these control signals. And so our offer here, Your Honor, is that it should be construed with that disclosure in mind.

But further to that, Your Honor, we have the disclaimer. And again, we cited this disclaimer with regard to this term. Netlist did not respond to it. Now, what we have here is for these terms, for the similar patent, Netlist said that the selective electrical coupling was a key contribution of the invention--not particular claim language, not a specific aspect of the invention, but the key contribution of the invention. And the clear black letter law from the Federal Circuit is when you make that kind of broad disclaimer, it applies to the later patents.

Now, there was a contention with regards to the 'buffer' terms that, Well, maybe the claim language didn't exactly line up. If you look at our briefing, Your Honor, you'll see that what the claim language at issue there was it was the question of how you enable, how you couple the memory devices to the data line. That was the issue in the claim language in the previous patent that was at issue in that Federal Circuit case, and that's the same exact issue here. And so for that case, they said the key contribution of the invention was the selective isolation that the -- this concept of selective isolation was essential to overcoming the shortcomings of the prior art modules. That was the module that didn't use the buffer to switch between one device or the other. And so here we have this disclaimer in that previous case that went unrebutted in Netlist's reply.

Thank you, Your Honor.

THE COURT: All right. Anything further from Plaintiff, Mr. Sheasby?

MR. SHEASBY: Your Honor, I will just be repeating what I said previously.

THE COURT: All right. We don't need that.

All right. We've got two more terms in dispute. I think there's merit in hearing argument on the two of them at the same time 'overall CAS latency' and 'wherein data transfers through the circuitry are registered for an amount of time delay'. These are both opposed -- or the issue is between Plaintiff and Micron only, not Samsung.

So let me hear argument from Netlist first, and then I'll hear argument from Micron.

MR. SHEASBY: Your Honor, the issue here is that the -- does 'CAS latency' only relate to read CAS latency or does it relate to both read and write CAS latency.

THE COURT: I understand that.

MR. SHEASBY: If it relates to both read and write, there is no indefiniteness, and I would say that there is substantial reason to believe that the language contemplates both read and write CAS latency.

The most trenchant example of this--I'm on slide 130--is that the claims contemplate both a read or write memory commands, and so the claims that discuss CAS latency are

claims that encompass both read and write memory commands. That's the case for the '417 Patent on slide 130. It's also the case for the '215 Patent on slide 131, because it says 'receive or output', and so that would be both the read and write command as opposed to just a read and write command.

Slide 132, the specification also makes clear that the design encompasses both read and write in dealing with latencies in the context of bode read and write. And Doctor Stone was shown the passage on CAS latency from the specification and he agreed that it could relate to both read and write transfers.

There is this odd sort of situation of which the Defendants are endorsing the use of the JEDEC specification to inform baseline terms in the claims. I'm not going to run away from that. I've asked you to do that as well, and so it is fair, just as I've asked you to look at the JEDEC specifications to define 'bit width' and the size of memory devices. I think it is fair to look at the JEDEC specification on 'CAS latency' as well. And what's clear is that 'CAS latency', as used in the JEDEC specification, encompasses both read and write latency. That's discussed at slide 136. So I'm --

THE COURT: If that's all true, then why is your offering here simply plain and ordinary meaning? Why don't you propose something that specifically defines what you're

now arguing to me?

MR. SHEASBY: You know, it's a fair criticism. We thought the claims say read or write in the claims. The body of the claims, in the previous limitations say read or write, and so we just think it's transparent that since it says read or write at the beginning of the claim and then afterwards it talks about data transfers that have a CAS latency, and a transfer would mean a read or write, there's no skulduggery involved.

We have no problem making clear that the data transfers include both read or write and the CAS latency is read or write. There was no desire at all to run away from that, Your Honor.

THE COURT: All right. Anything further on either of these two terms?

MR. SHEASBY: No, that's it for me. Thank you, Your Honor.

THE COURT: Let me hear a response from Micron, please.

MR. RUECKHEIM: Your Honor, Mike Rueckheim again.

THE COURT: Please proceed.

MR. RUECKHEIM: There is no dispute that the claims recite -- I think it's the memory module that can send or receive read and write commands. That has nothing to do with the claim language at present here.

Counsel said something to the effect that JEDEC uses read and write CAS latency. That's false. The documents that were just shown to the Court talk about read latency, talked about write latency, and it talked about CAS latency. That's the claim language here--'CAS latency'.

And with respect to this claim language, Your Honor is exactly right. This -- the claim language on the screen, this is I think the toughest technology-wise most complex as far as for the jury to understand, and just grammatically. It says the memory module has an overall CAS latency. It says the actual operation CAS latency of memory integrated circuits--two different things.

We need a construction here, and so what we did is we asked our expert, What does this term mean. We looked at the JEDEC spec--what does this term mean, and when you're talking about overall CAS latency of a module, you're talking about the delay between when a read command is executed on the -- by the module and when the module -- you think of a card with memory devices on it. The computer sends it a read command; boom, it gets it, that's your start time. You get your memory devices on there, they're going to go get the data, shoot it back out the card to the computer. That's the end time. That's your delay.

When you go to the actual operational CAS latency, you're now talking about the integrated circuits. That's what the

claim says. It's not talking about the module anymore. And so it's when the integrated circuits on your module receive your command and then execute that command and get the data from the memory and then shoot it back. That's the main distinction here.

And so why did we look at JEDEC? Why did we talk to the expert? The specification is silent. There's no description. This is a complex term. The jury needs a construction here. And so we looked at extrinsic evidence, we looked at expert analysis, because the specification tells us nothing.

This slide is just really just talking about why JEDEC is relevant. The slide from JEDEC is on the screen. It discusses read latency in terms of the CAS latency plus one, the register that's on the DIMM. The top section there from JEDEC, it talks about a read latency is the day between when the module gets the read command and the availability of the first piece of data on the output.

So we're not trying to say 'CAS latency' excludes write commands at all. It's not. It's a different term. But it's defined whet the module actually receives something for overall of the module and then sends that data back out, and it's defined separately when you're talking about the integrated circuits.

Why that's important is because the claim language does a comparison of the overall CAS latency. It says it has to be

greater--this is talking about the registered data transfers--adds this delay such that the overall CAS latency of the module is greater than that of the operational CAS latency. Here it's the memory devices, but it means the memory integrated circuits on the module. And so that leads to the problem.

So we're not trying to exclude -- 'CAS latency' is a stand-alone term. It's used all the time with respect to read and write commands. It's just the delay for read command when the module gets the command and then sends it back out. Write command is defined -- write latency--I'm sorry--not the write CAS latency. That's not a term. Write latency is defined as a sub-pact of that.

But the problem becomes is that the language the Court pointed to, is that the claim says you have data transfers through the circuitry that are transferred -- that are registered--I'm sorry--for an amount of time such as this relationship happens. The overall module latency is greater than the device latency.

So the problem with that is under Micron's view, really 'CAS latency' is only referring to when you have a read command come in and then a delay until the data gets kicked back out, and -- but the claim says it write commands, too. And so if a write command is being registered through, there's no way a write command could ever be registered through a

module such that it affects the read. They just -- they're two independent -- apples and oranges, Your Honor.

And then we get to Netlist's proposal. And this is why -- despite the indefiniteness argument, this is why we need a construction for this term, because Netlist in another proceeding said this term means the delay between when a command is sampled on the memory module and when the first piece of data is available at the pins. So they said that in a separate proceeding, but in this proceeding they said, No, that was a separate proceeding; we're not taking that position here.

So if they think we're wrong, tell us why, and the jury's going to have to do an analysis here and they don't know what these terms mean. I think it's highly unlikely -- I don't want to talk bad about the potential jury here, but I think it's very complex terminology. And even under Netlist's view, the delay for a write command coming in and when the write data is available at the module pins is zero. The write data and command come in at the exact same time, and there's no way the rest of the claim makes sense. When the overall CAS latency is zero, that can't be greater than anything else, no matter how long you register.

THE COURT: All right.

MR. RUECKHEIM: Thank you, Your Honor.

THE COURT: Anything further from Plaintiff?

MR. SHEASBY: I would just be repeating myself, Your Honor.

THE COURT: All right. Well, those appear to be all the terms scheduled for claim construction today, counsel. I appreciate your time and your argument. Except for the one term that the parties agreed for the Court to decide on the briefing, I've heard your arguments and will consider those further in light of the briefing. And I'll do my best to get you a written claim construction order as soon as practical. I can't give you an exact date on that, but I will get to it as quickly as can.

As I say, I appreciate your argument today. That completes the presentation regarding claim construction in both the Samsung and the Micron cases, as cited in the record. You're excused.

And the Court stands in recess. Thank you.

(End of hearing.)

I HEREBY CERTIFY THAT THE FOREGOING IS A CORRECT TRANSCRIPT FROM THE RECORD OF PROCEEDINGS IN THE ABOVE-ENTITLED MATTER. I FURTHER CERTIFY THAT THE TRANSCRIPT FEES FORMAT COMPLY WITH THOSE PRESCRIBED BY THE COURT AND THE JUDICIAL CONFERENCE OF THE UNITED STATES.

S/Shawn McRoberts 09/30/2023

_____DATE_____
SHAWN McROBERTS, RMR, CRR
FEDERAL OFFICIAL COURT REPORTER